

Model Name : B5/B7W1A  
File Name : LA-D641P

# Compal Confidential

## B5/B7W1A M/B Schematics Document

Intel Apollo lake  
UMA

2016-07-22

REV:1.A

For 1A PCB

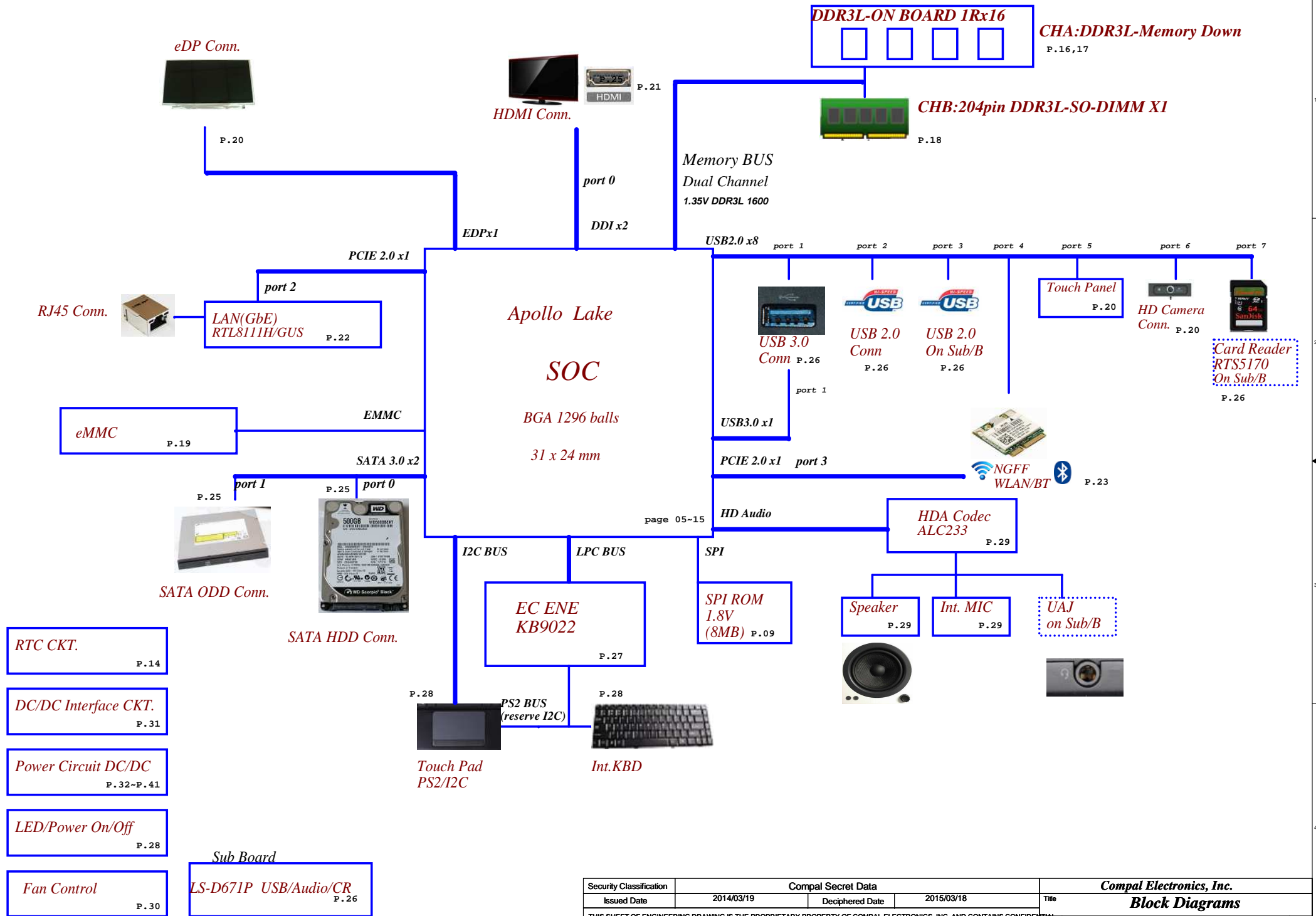
PCB15A@ ZZZ	
Part Number	Description
DA6001K401A	PCB 1NU LA-D641P REV1A MB 1

PCB17A@ ZZZ3	
Part Number	Description
DA6001K411A	PCB 1NU LA-D641P REV1A MB 2

PCB15@ ZZZ	
Part Number	Description
DA6001K4000	PCB 1NU LA-D641P REV0 MB 1

PCB17@ ZZZ	
Part Number	Description
DA6001K4100	PCB 1NU LA-D641P REV0 MB 2

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Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title	Cover Page
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Power Plane	Description	S0	S3	S4/S5
+19V_VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
+19VB	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	OFF
+1.8VALW	+1.8v Always power rail	ON	ON	OFF
+3V_SOC	+3v Always power rail for SOC	ON	ON	OFF
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	ON
+3V_PTP	+3.3V power rail for PTP	ON	ON	OFF
+VNN	other (non core) logic voltage for SOC	ON	OFF	OFF
+VCC_VCGI	Core & GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.05VS	+1.05v System power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.  
Note : ON\*\* dGPU optimus on

EC	Power	BAT	CHGR	NGFF
EC_SMB_CK1 EC_SMB_DA1	+3VALW	V	V	X
EC_SMB_CK2 EC_SMB_DA2	+3VS	X	X	V

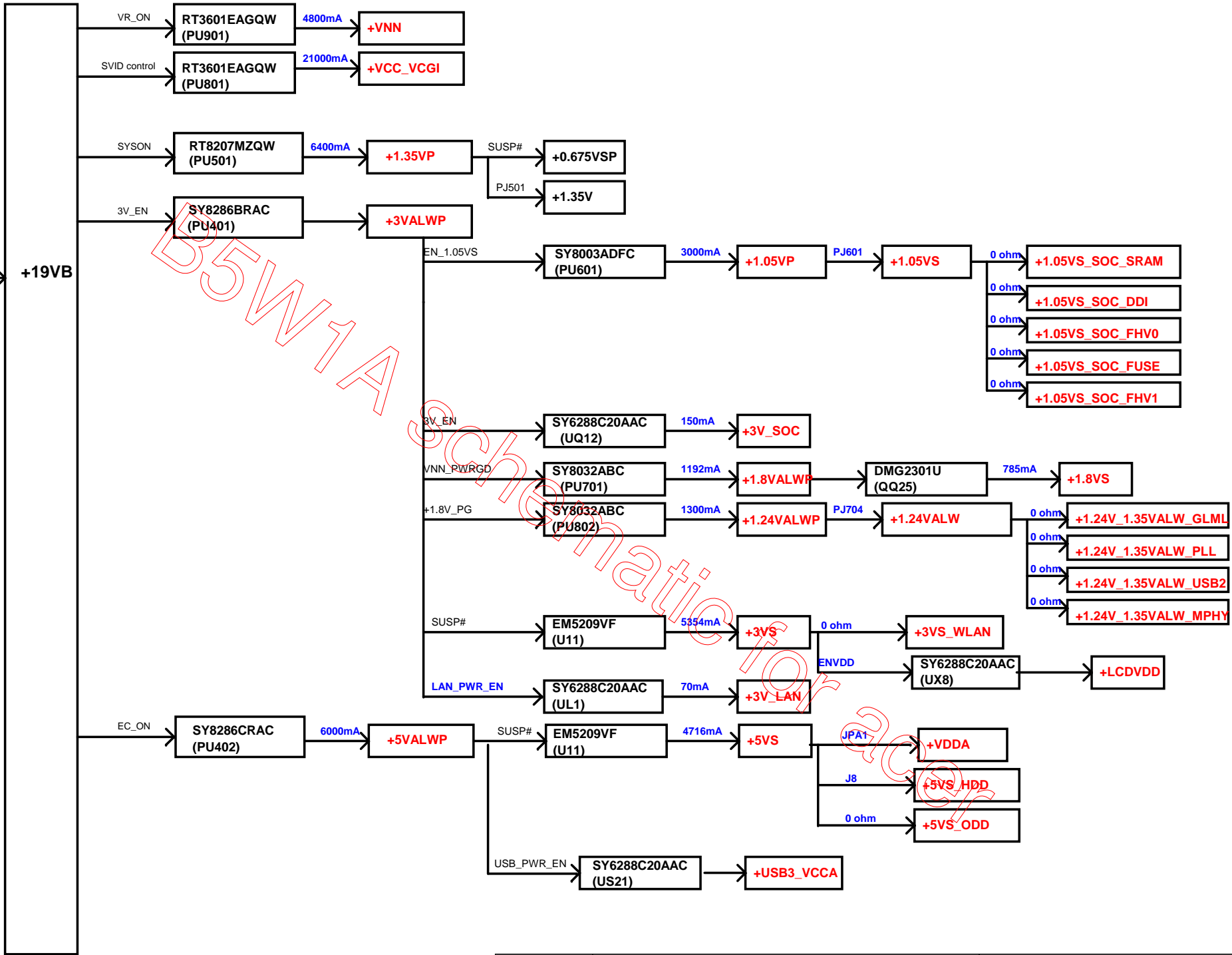
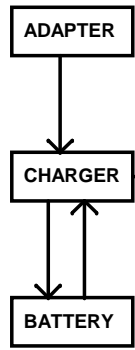
SOC	Power	DIMM1	DIMM2
SMB Address			
SOC_SMBCLK SOC_SMBDATA	+3VS	V	V

	Power	Touch PAD	Touch Panel
I2C Address		0xXX	0xXX
I2C Port3	+1.8VALW to +TS_PWR	X	V
I2C Port4	+1.8VALW to +3V_PTP	V	X

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00-0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14-0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F-0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26-0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31-0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B-0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46-0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55-0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65-0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77-0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88-0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97-0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5-0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0-0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8-0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0-0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA-0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5-0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE-0xF0
19	NC	3.000V	3.000V		0xF1-0xFF

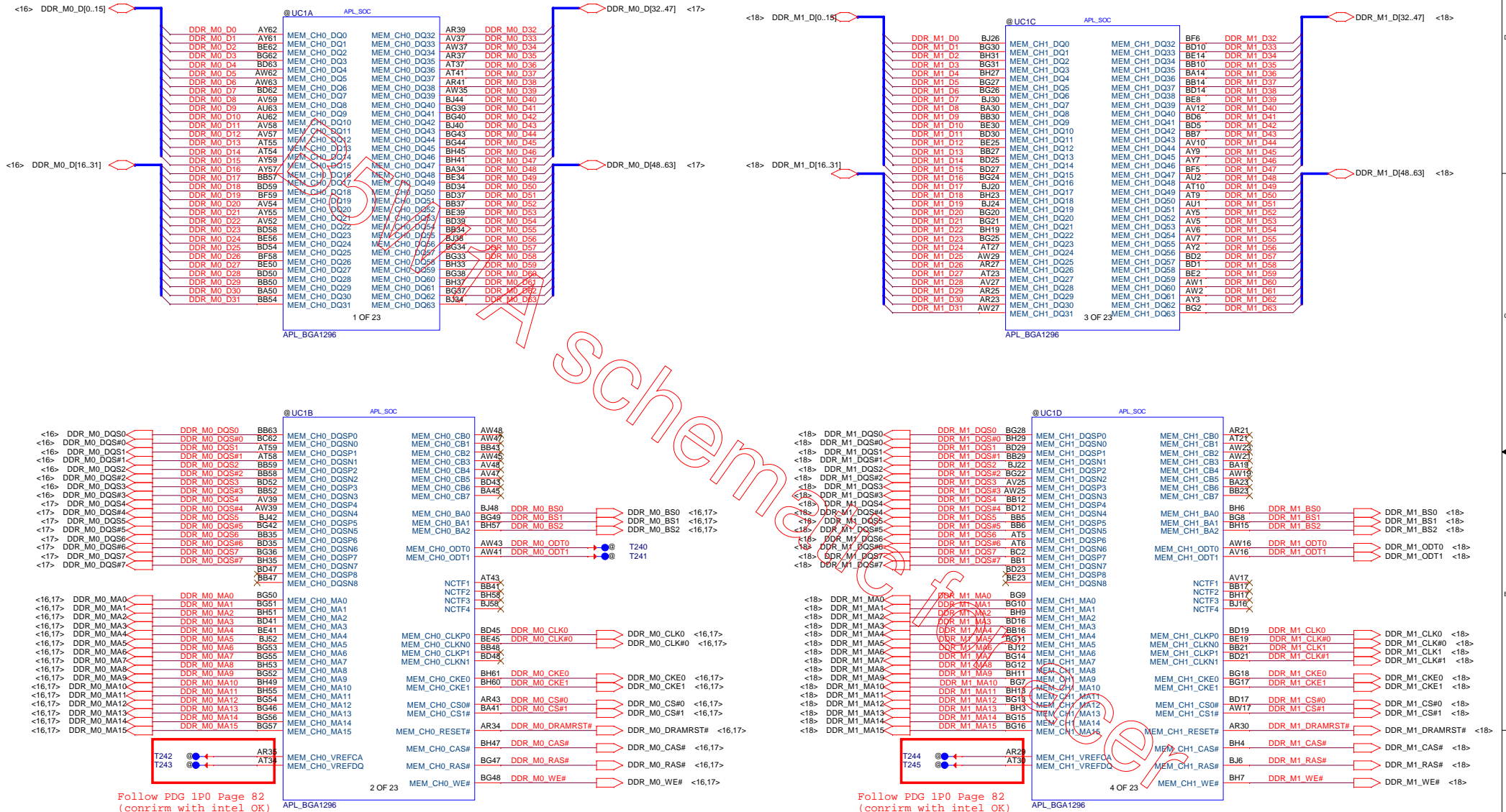
43 Level	Description	BOM Structure
431A2BB0L07	SMT MB AD641 B5W1A QKT4 HDMI	233e/8111H0/NBYOC0/CMC0/PCB150/QKT40
431A2BB0L08	SMT MB AD641 B5W1A QKTY 2G HDMI	233e/8111H0/NBYOC0/CMC0/PCB150/QKTY0/MD0
431A2BB0L09	SMT MB AD641 B5W1A QKTW 2G HDMI	233e/8111H0/NBYOC0/CMC0/PCB150/QKTW0/MD0
431A2BB0L60	SMT MB AD641 B7W1A QKT4 HDMI	233e/8111H0/NBYOC0/CMC0/PCB170/QKT40
431A2BB0L61	SMT MB AD641 B7W1A QKT4 2G HDMI	233e/8111H0/NBYOC0/CMC0/PCB170/QKT40/MD0
431A2BB0L62	SMT MB AD641 B7W1A QKTY 2G HDMI	233e/8111H0/NBYOC0/CMC0/PCB170/QKTY0/MD0
431A2BB0L63	SMT MB AD641 B7W1A QKTW 2G HDMI	233e/8111H0/NBYOC0/CMC0/PCB170/QKTW0/MD0

Board ID	PCB Revision
01	EVT_LA-D641PR01
02	DVT_LA-D641PR02
03	PVT(DVT2)_LA-D641PR03
04	Pre MP_LA-D641PR10
05	Pre MP_LA-D641PR1A





# Non-Interleaved Memory



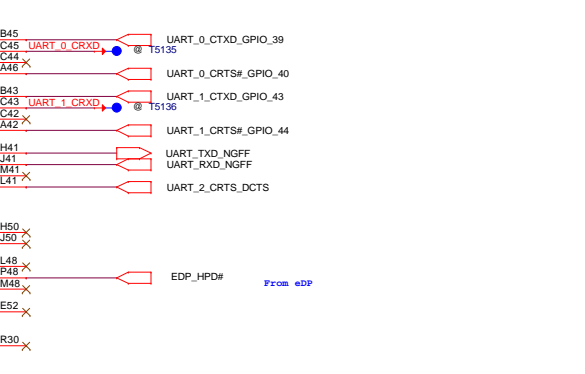
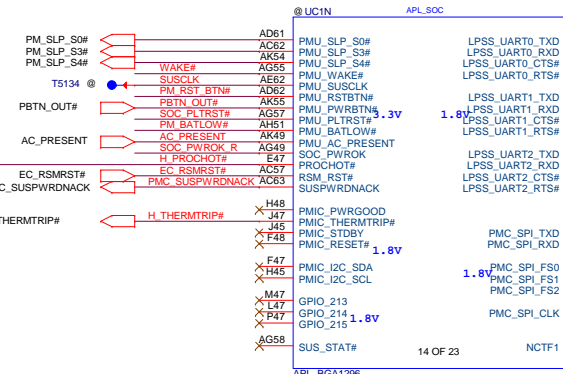
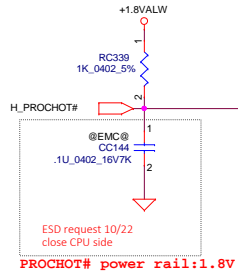
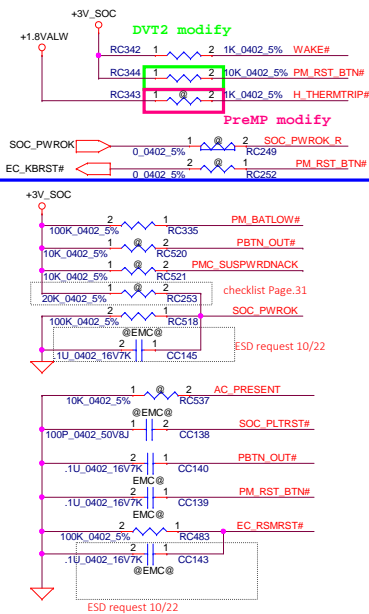
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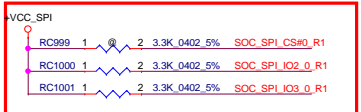
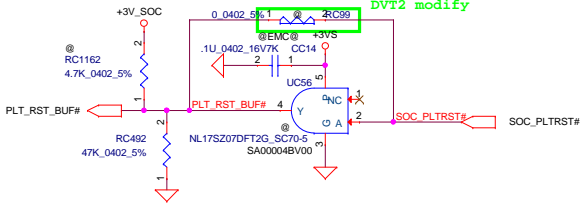






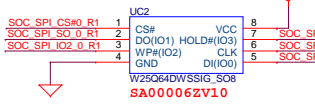
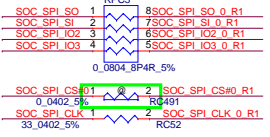


PDG0p7 P.34 PLTRST# V1P8/V3P3(The I/O voltage selection is done by using Hardware Strap GPIO\_88)



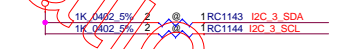
Need to check Follow CRB 0.9 P.65

8M SPI ROM(Support ISH)

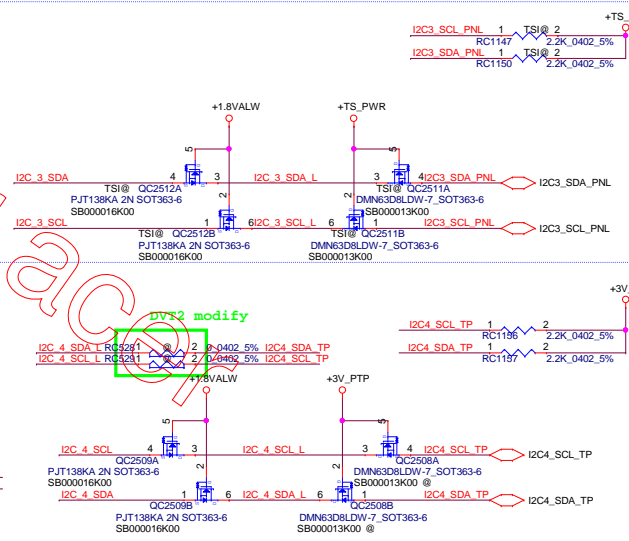
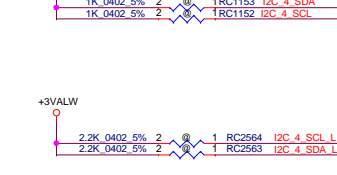


EMI request 11/03

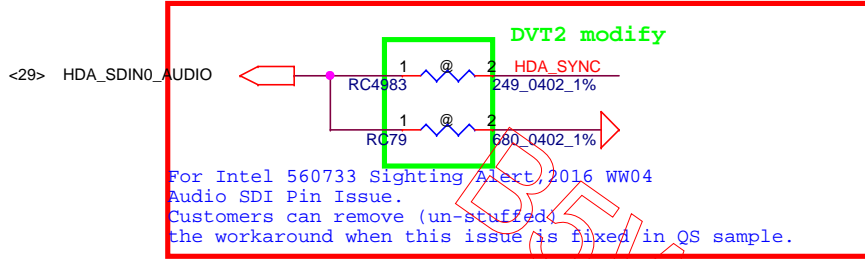
For Touch Screen



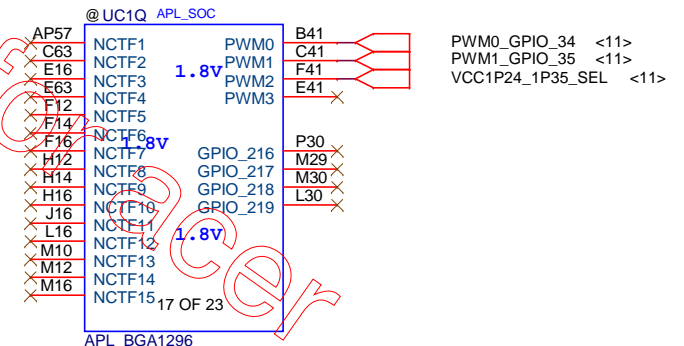
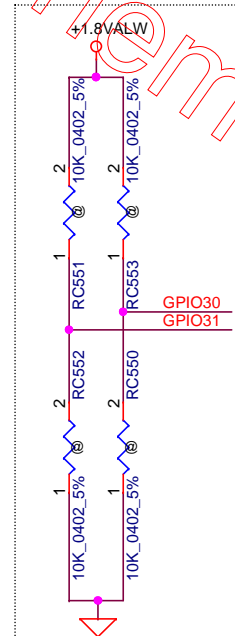
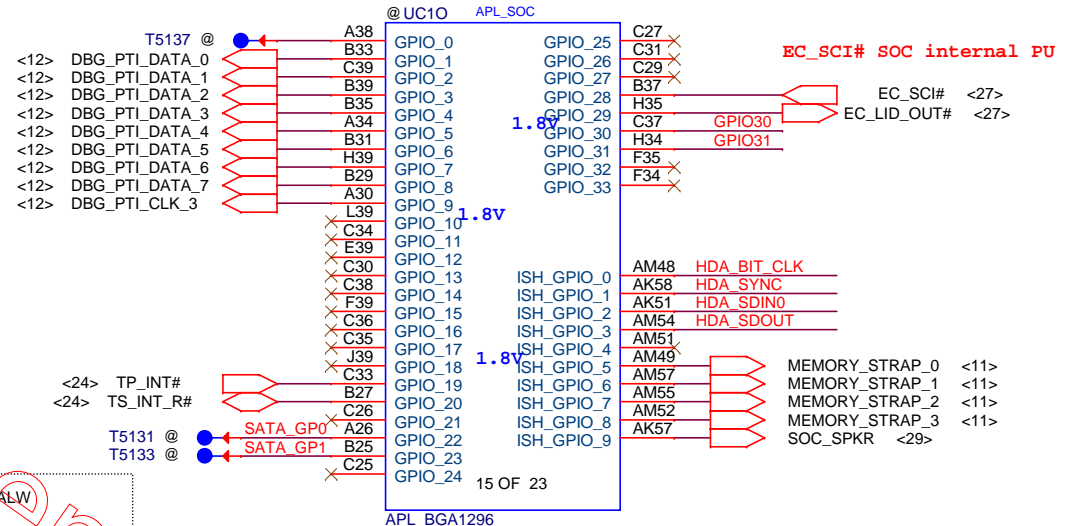
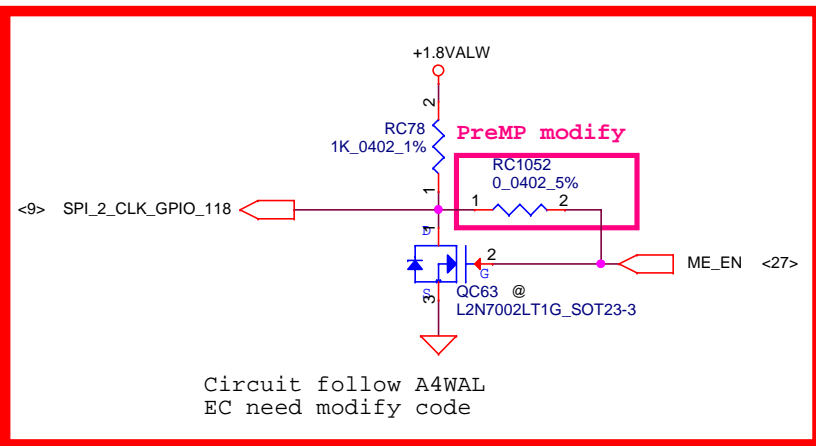
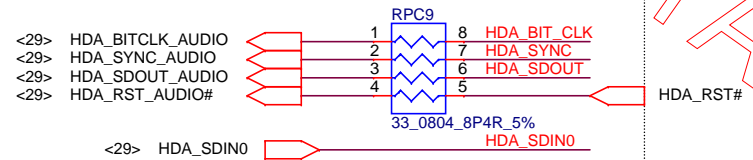
For Touch Pad



Intel HDA issue, Fix on QS sample 09/01

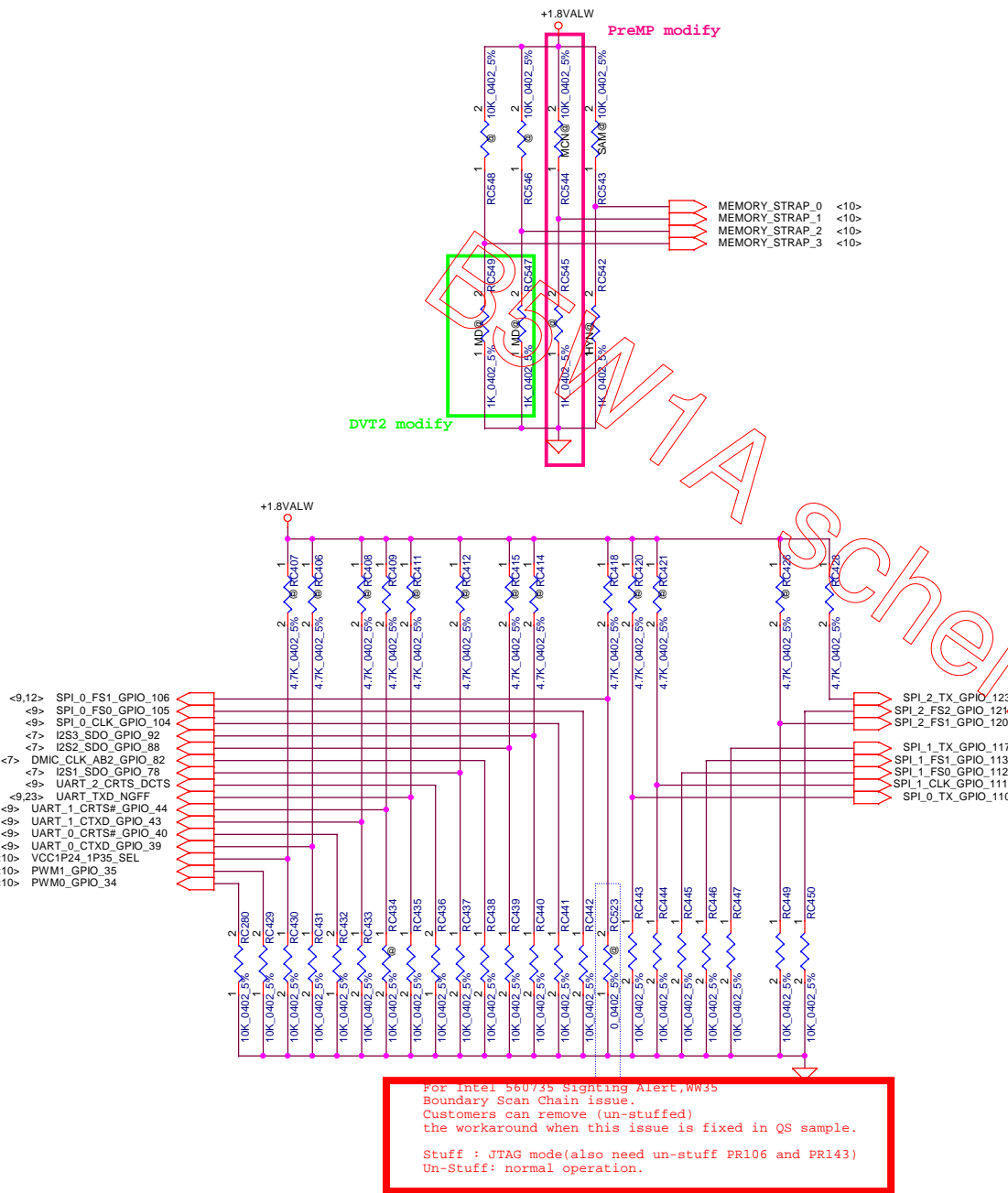


### HDA for AUDIO



SW request 1104

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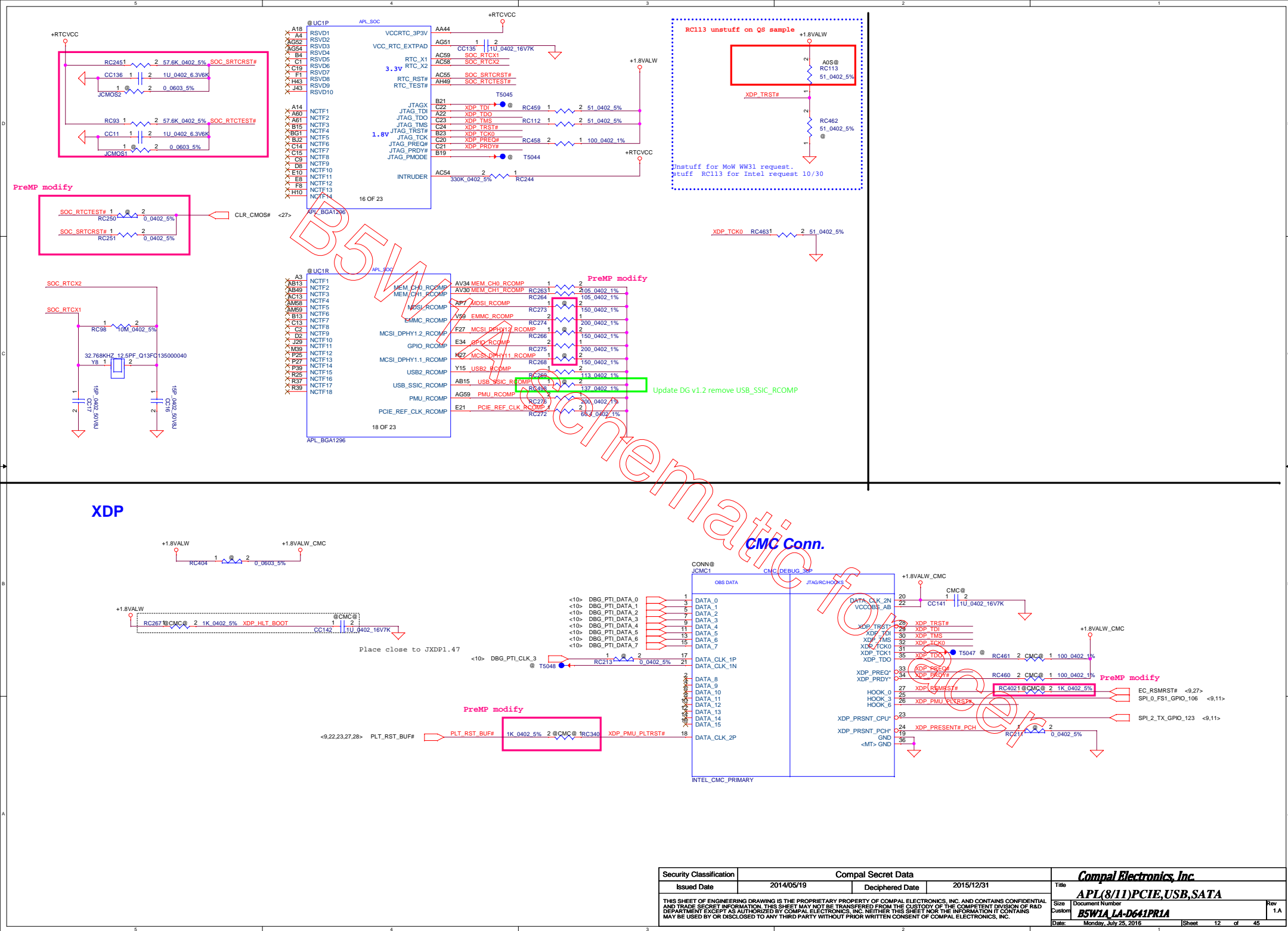


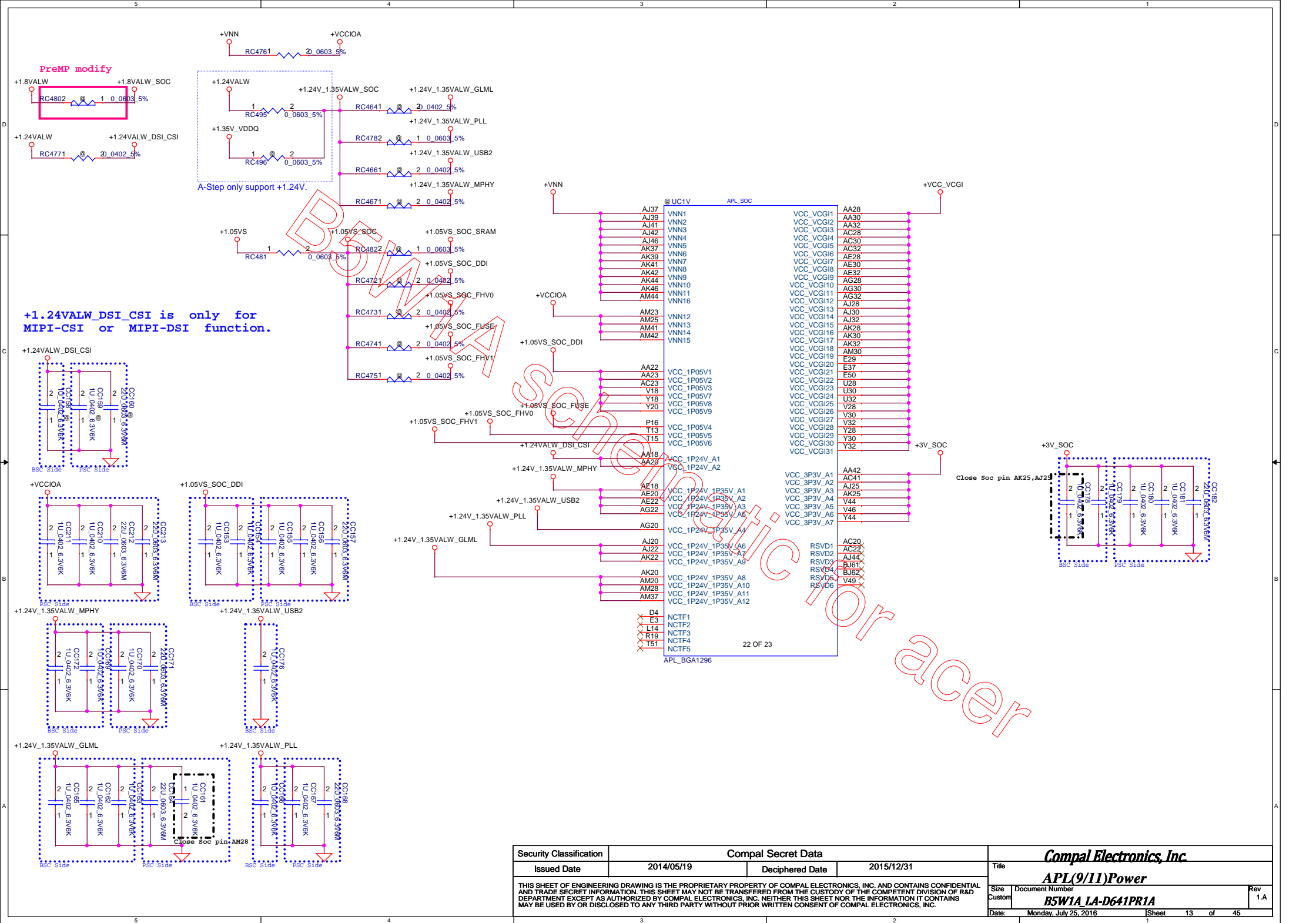
# On Board Memory Strap Pin

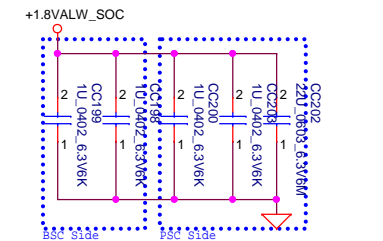
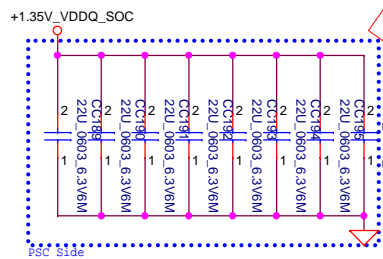
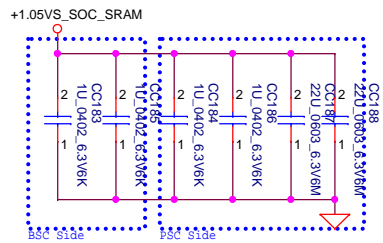
On Board RAM Configuration	RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0
DDR3L Hynix 256MX16/1600 H5TC4G63CFR-PBA (SA00005AVD0)	0	0	0	0
DDR3L Samsung 256MX16/1600 K4B4G1646E-BYK0 (SA000099X20)	0	0	0	1
DDR3L Micron 256MX16/1600 MT41K256M16TW(SA00009KQ30)	0	0	1	0
SODIMM only	1	1	1	1

\* stand for default value

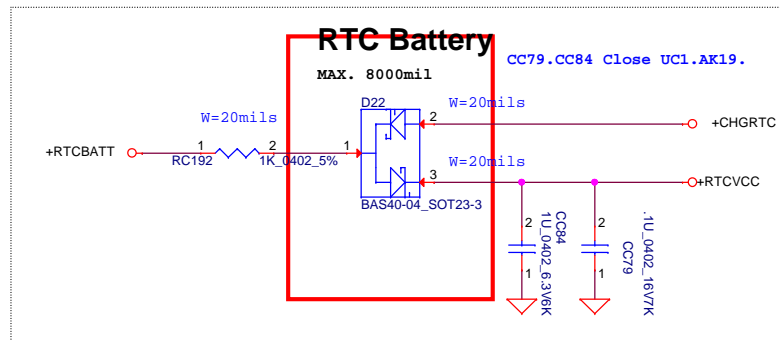
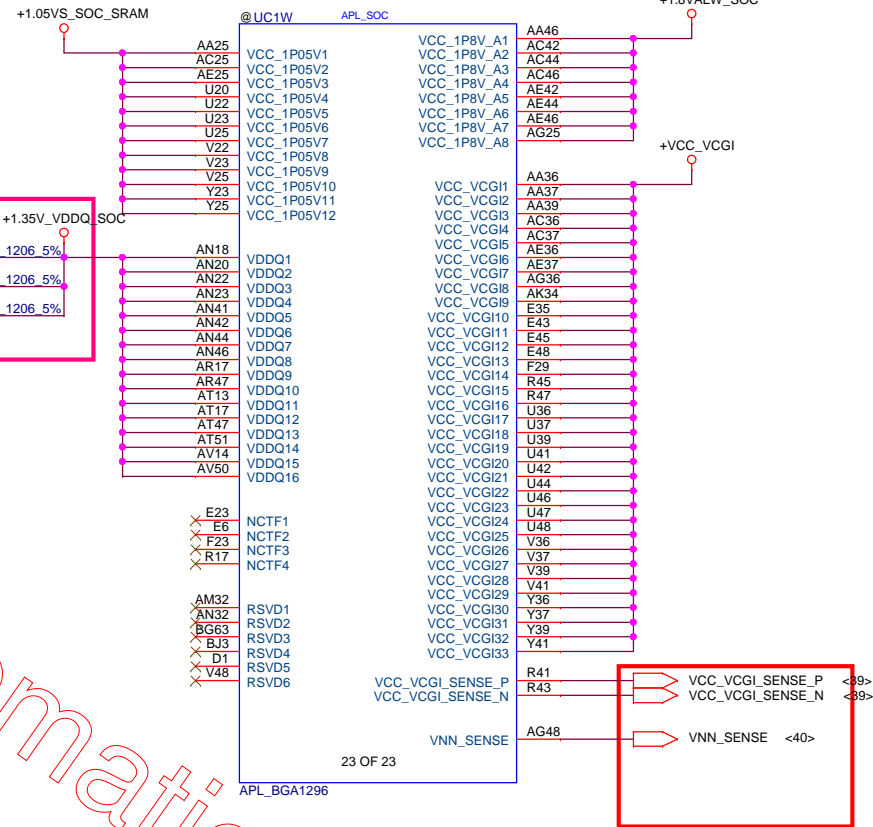
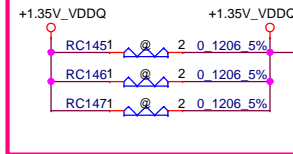
Pin Name	PU/PD Function	External Termination	Strap pin Description
GPIO34		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO35		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO36	0: 1.24V* 1: 1.35V	10KPD	VCC_1P24V_1P35V_A voltage selection
GPIO39	0: Disable* 1: Enable	10KPD	Enable CSE ROM Bypass
GPIO40		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO43	0: Disable* 1: Enable	4.7KPU	Allow eMMC as a boot source
GPIO44	0: Disable 1: Enable*	4.7KPU	Allow SPI as a boot source
GPIO47	0: No Force* 1: Force	10KPD	Force DNX FW Load
GPIO48		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO78	0: 3.3V* 1: 1.8V	10KPD	SMBus 1.8V/3.3V mode select
GPIO82		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO85	0: 3.3V* 1: 1.8V	10KPD	PMU 1.8V/3.3V mode select
GPIO92	0: Disable* 1: Enable	10KPD	SMBus No Re-Boot
GPIO104		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO105		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO106		4.7KPU	Pulled HIGH when RSM_RST_N de-asserts
GPIO110	0: 3.3V* 1: 1.8V	10KPD	LPC 1.8V/3.3V mode select
GPIO111	0: From SPI* 1: Don't	10KPD	Boot BIOS from SPI select
GPIO112		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO113		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO117		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO118	0: Don't* 1: Override	10KPD	Flash Descriptor Override
GPIO120	0: Enable* 1: Disable	10KPD	Top swap override
GPIO121		10KPD	Pulled LOW when RSM_RST_N de-asserts
GPIO123		4.7KPU	Pulled HIGH when RSM_RST_N de-asserts







PreMP modify



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@UC1S APL_SOC		
AG42	VSS70	VSS1
AG44	VSS71	VSS2
AG46	VSS72	VSS3
AH15	VSS73	VSS4
AH16	VSS74	VSS5
AH48	VSS75	VSS6
AH5	VSS76	VSS7
AH52	VSS77	VSS8
AH54	VSS78	VSS9
AH55	VSS79	VSS10
AH57	VSS80	VSS11
AH58	VSS81	VSS12
AH59	VSS82	VSS13
AH6	VSS83	VSS14
AH7	VSS84	VSS15
AJ1	VSS85	VSS16
AJ18	VSS86	VSS17
AJ2	VSS87	VSS18
AJ23	VSS88	VSS19
AJ27	VSS89	VSS20
AJ34	VSS90	VSS21
AJ36	VSS91	VSS22
AJ63	VSS92	VSS23
AK10	VSS93	VSS24
AK12	VSS94	VSS25
AK18	VSS95	VSS26
AK23	VSS96	VSS27
AK27	VSS97	VSS28
AK48	VSS98	VSS29
AK5	VSS99	VSS30
AK52	VSS100	VSS31
AK59	VSS101	VSS32
AK9	VSS102	VSS33
AM18	VSS103	VSS34
AM22	VSS104	VSS35
AM27	VSS105	VSS36
AM34	VSS106	VSS37
AM36	VSS107	VSS38
AM39	VSS108	VSS39
AM46	VSS109	VSS40
AN1	VSS110	VSS41
AN10	VSS111	VSS42
AN11	VSS112	VSS43
AN13	VSS113	VSS44
AN14	VSS114	VSS45
AN16	VSS115	VSS46
AN17	VSS116	VSS47
AN2	VSS117	VSS48
AN25	VSS118	VSS49
AN27	VSS119	VSS50
AN28	VSS120	VSS51
AN30	VSS121	VSS52
AN34	VSS122	VSS53
AN36	VSS123	VSS54
AN37	VSS124	VSS55
AN39	VSS125	VSS56
AN47	VSS126	VSS57
AN48	VSS127	VSS58
AN5	VSS128	VSS59
AN50	VSS129	VSS60
AN51	VSS130	VSS61
AN53	VSS131	VSS62
B63	VSS132	VSS63
		VSS64
		VSS65
		VSS66
		VSS67
		VSS68
		VSS69

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PAG Op91 Page22  
VNN\_VSS\_SENSE point should locate at  
remote APL SOC GND pin AE47 or AE48.

@UC1T APL_SOC		
AK36	VSS1	VSS70
AK19	VSS2	VSS71
AK32	VSS3	VSS72
AK45	VSS4	VSS73
AT12	VSS5	VSS74
AT16	VSS6	VSS75
AT19	VSS7	VSS76
AT2	VSS8	VSS77
AT25	VSS9	VSS78
AT29	VSS10	VSS79
AT3	VSS11	VSS80
AT35	VSS12	VSS81
AT39	VSS13	VSS82
AT45	VSS14	VSS83
AT48	VSS15	VSS84
AA1	VSS16	VSS85
AT57	VSS17	VSS86
AT61	VSS18	VSS87
AT62	VSS19	VSS88
AT7	VSS20	VSS89
AU32	VSS21	VSS90
AV19	VSS22	VSS91
AV2	VSS23	VSS92
AV21	VSS24	VSS93
AV23	VSS25	VSS94
AV29	VSS26	VSS95
AV3	VSS27	VSS96
AV32	VSS28	VSS97
AV35	VSS29	VSS98
AV41	VSS30	VSS99
AV43	VSS31	VSS100
AV45	VSS32	VSS101
AV55	VSS33	VSS102
AV61	VSS34	VSS103
AV62	VSS35	VSS104
AV9	VSS36	VSS105
AW14	VSS37	VSS106
AW30	VSS38	VSS107
AW34	VSS39	VSS108
AW50	VSS40	VSS109
AY10	VSS41	VSS110
AY32	VSS42	VSS111
AY64	VSS43	VSS112
AY58	VSS44	VSS113
AY6	VSS45	VSS114
B2	VSS46	VSS115
B3	VSS47	VSS116
B62	VSS48	VSS117
B9	VSS49	VSS118
BA1	VSS50	VSS119
BA12	VSS51	VSS120
BA16	VSS52	VSS121
BA17	VSS53	VSS122
BA2	VSS54	VSS123
BA21	VSS55	VSS124
BA25	VSS56	VSS125
BA27	VSS57	VSS126
BA29	VSS58	VSS127
BA32	VSS59	VSS128
BA35	VSS60	VSS129
BA37	VSS61	
BA39	VSS62	
BA43	VSS63	
BA47	VSS64	
BA48	VSS65	
BA52	VSS66	
BA62	VSS67	
BA63	VSS68	
BB19	VSS69	

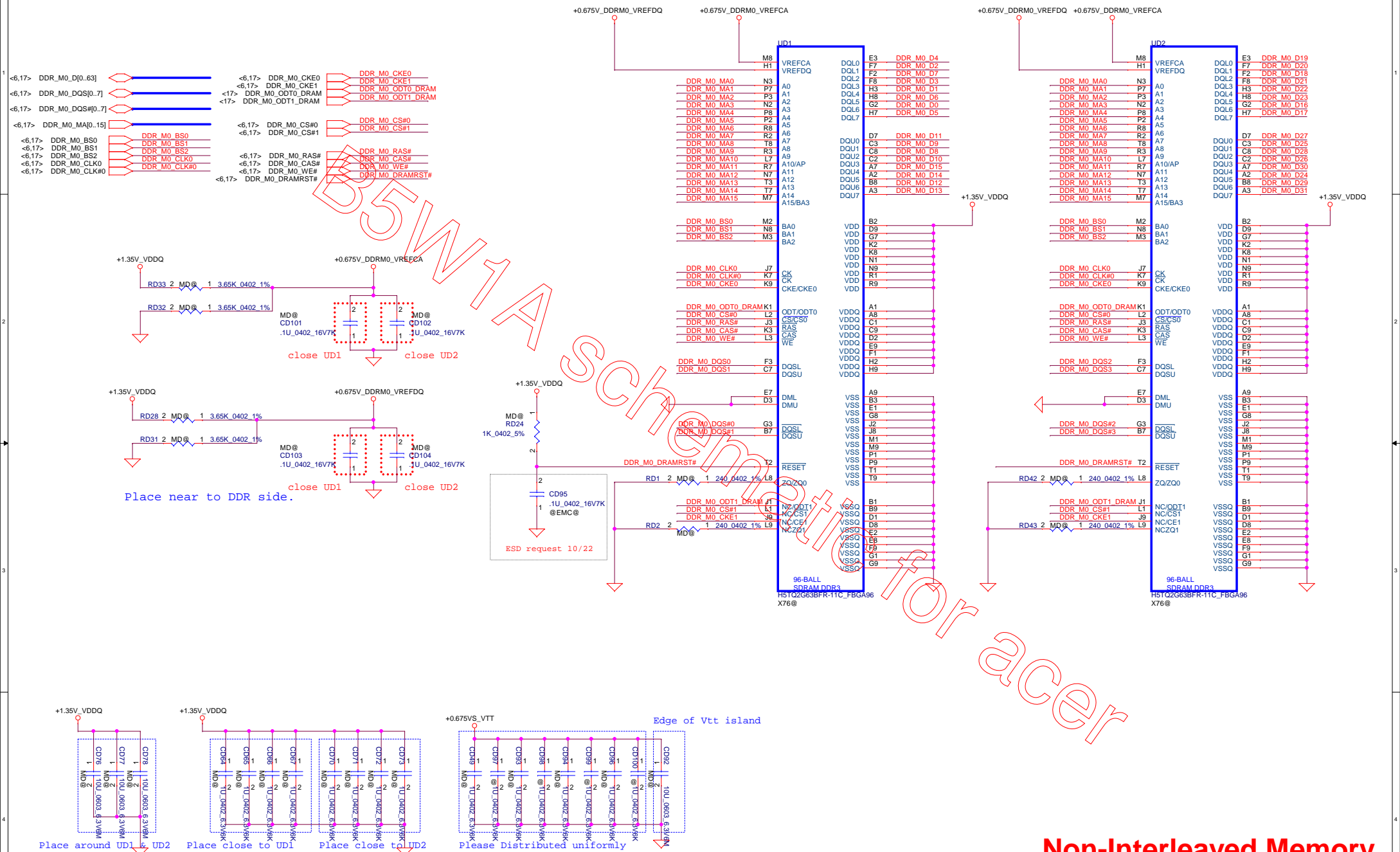
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APL\_BGA1296

@UC1U APL_SOC		
AN54	VSS1	M32
AN56	VSS2	M50
AN57	VSS3	M59
AN59	VSS4	M5
AN63	VSS5	N1
AN7	VSS6	N32
AN8	VSS7	N63
AP55	VSS8	P13
AP9	VSS9	P19
C28	VSS10	P35
C32	VSS11	P37
C40	VSS12	P41
C48	VSS13	P43
D32	VSS14	P45
D58	VSS15	P5
D6	VSS16	P59
E12	VSS17	P9
E14	VSS18	R23
E19	VSS19	R29
E27	VSS20	R32
E4	VSS21	T49
F10	VSS22	U1
F21	VSS23	U10
F3	VSS24	U11
F32	VSS25	U13
F37	VSS26	U14
F45	VSS27	U16
F46	VSS28	U17
F50	VSS29	U18
F56	VSS30	U2
F59	VSS31	U27
F63	VSS32	U34
G1	VSS33	U5
G32	VSS34	U50
H17	VSS35	U51
H23	VSS36	U53
H29	VSS37	U54
H3	VSS38	U56
H37	VSS39	U57
H47	VSS40	U59
H61	VSS41	U62
H7	VSS42	U63
J12	VSS43	U7
J14	VSS44	U8
J19	VSS45	V20
J27	VSS46	V27
J30	VSS47	V34
J32	VSS48	V42
J35	VSS49	V48
J37	VSS50	V48
J48	VSS51	V5
J63	VSS52	V52
K32	VSS53	V54
K54	VSS54	V55
K55	VSS55	V57
K57	VSS56	V59
K6	VSS57	V6
L21	VSS58	V62
L27	VSS59	V64
L29	VSS60	V65
L36	VSS61	V67
L43	VSS62	V69
L45	VSS63	V7
L50	VSS64	V7
M14	VSS65	VSS134
M27	VSS66	
M3	VSS67	
M3	VSS68	
M3	VSS69	

21 OF 23  
APL\_BGA1296

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				Document Number	BSW1A LA-D641PR1A
				Date	Monday, July 25, 2016
				Sheet	15 of 45
				Rev	1.A

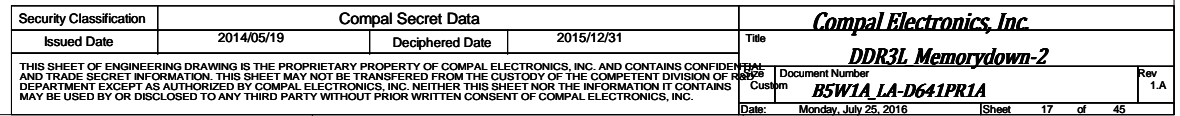
## CH0 DDR3L Memory Down Lower Bits



## Non-Interleaved Memory

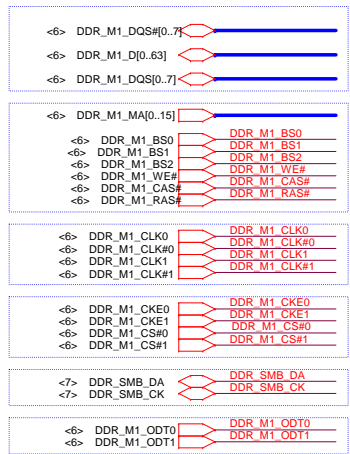
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Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title <b>B5W1A LA-D641PR1A</b>	Rev 1.A
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Date: Monday, July 25, 2016				Sheet 16 of 45	

## Non-Interleaved Memory



# Normal Type

## 2-3A to 1 DIMMs/channel



D/Q Signals link to CPU

CMD Signals from CPU

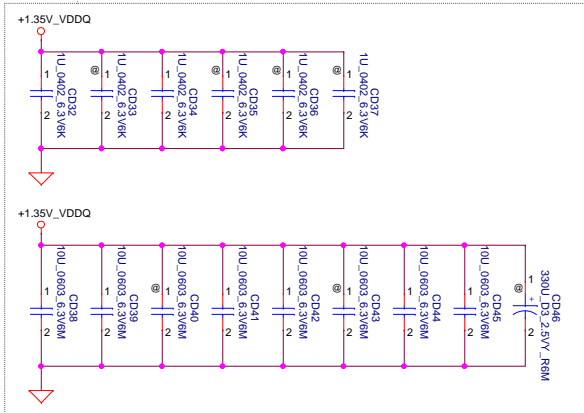
Clock Signals from CPU

CTL Signals from CPU

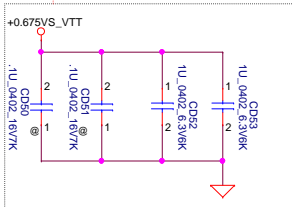
SMBUS signals link to CPU

From SOC ODT Signals to CH B

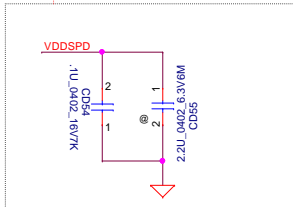
Layout Note:  
Place near JDIMM2



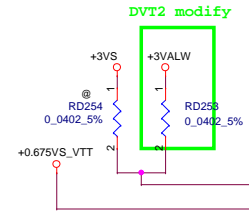
Layout Note:  
Place near JDIMM2.203,204



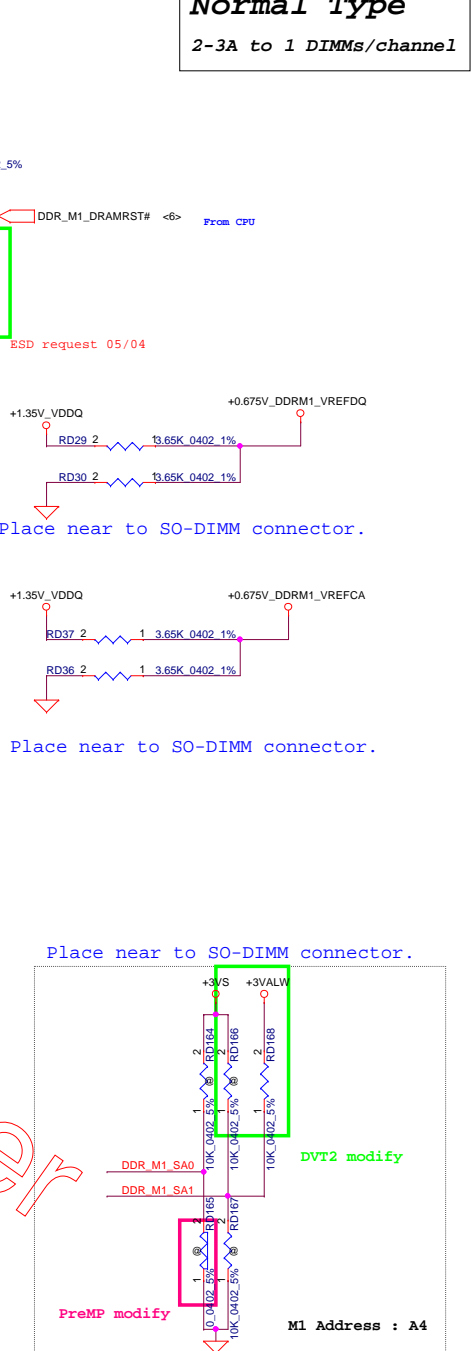
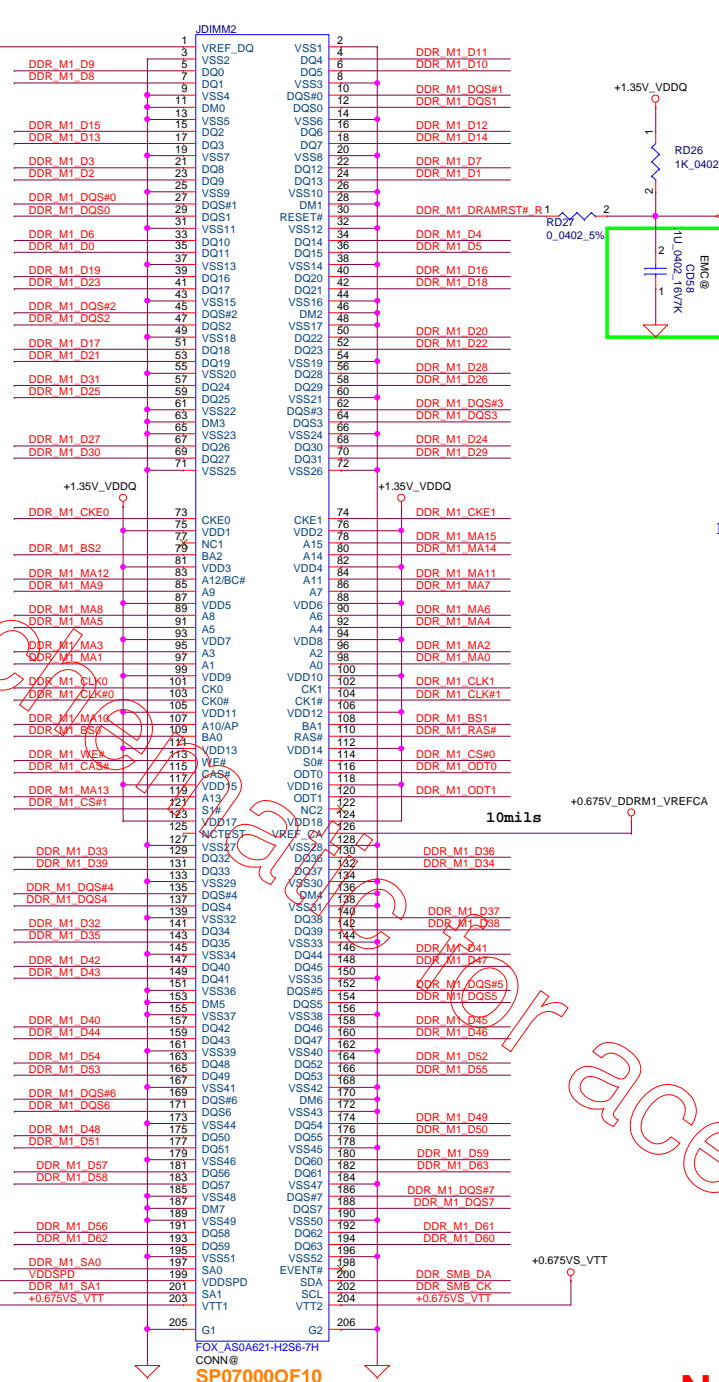
Layout Note:  
Place near JDIMM2.199



EMI request 11/03



DVT2 modify

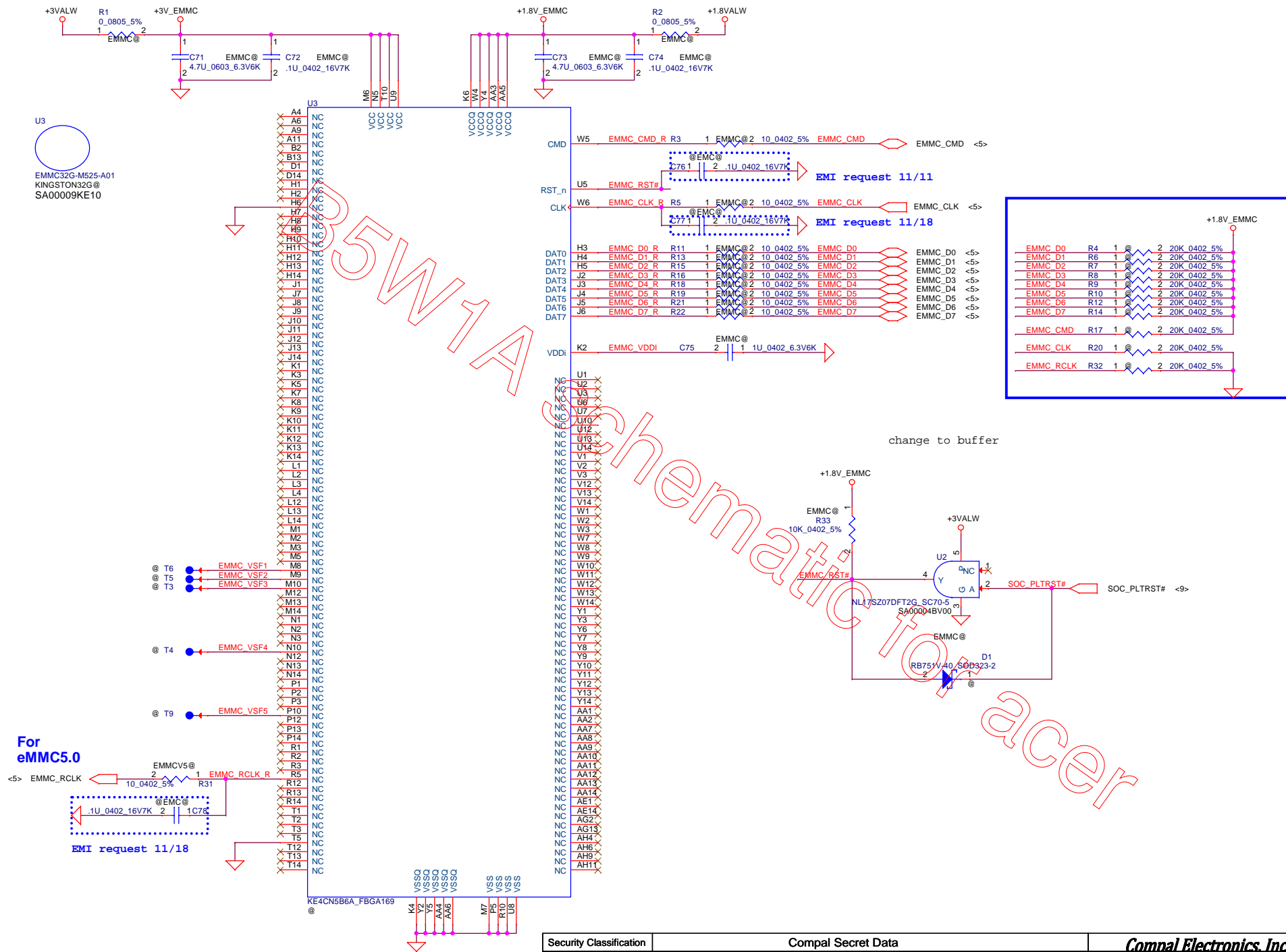


PreMP modify

M1 Address : A4

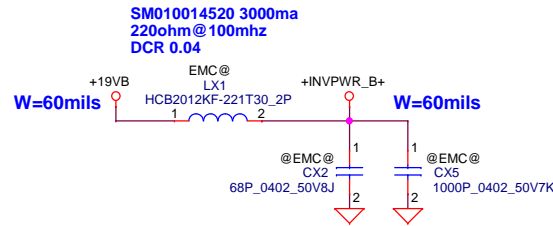
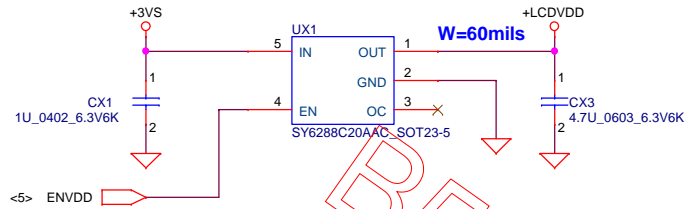
# Non-Interleaved Memory

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				B5W1A 1A-D641PR1A	1.A
				Date: Monday, July 25, 2016	Sheet 18 of 45

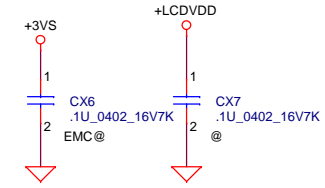


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date	Monday, July 25, 2016
				Sheet	19 of 45

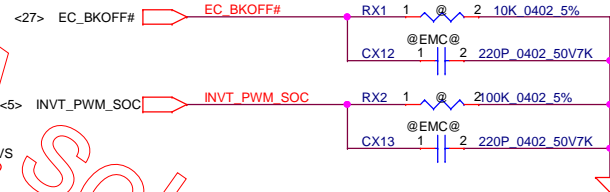
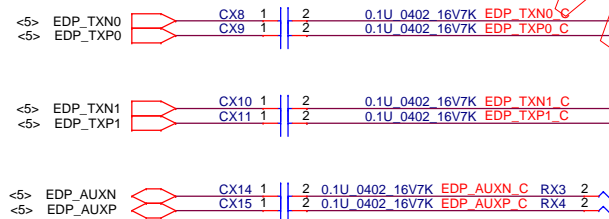
## LCD POWER CIRCUIT



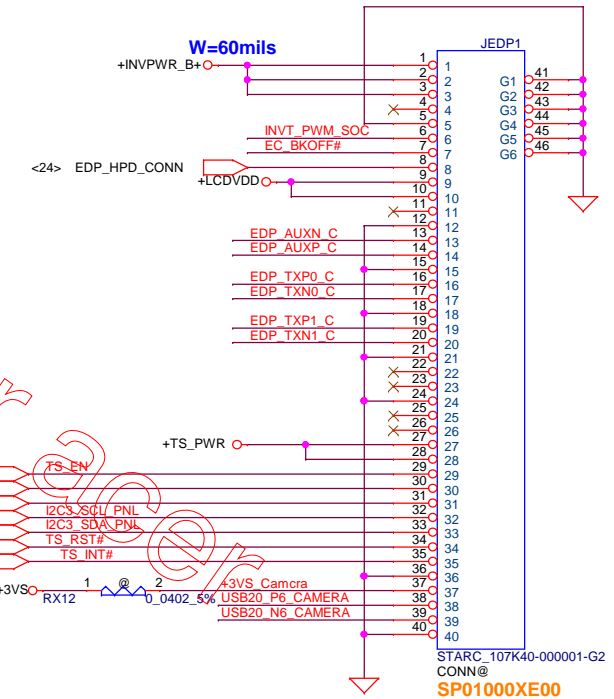
## Place closed to JEDP1



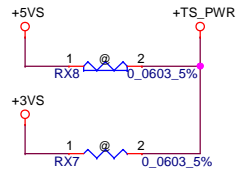
## eDP



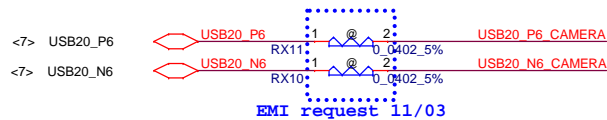
## LCD/ LED PANEL Conn.



## For Touch Panel



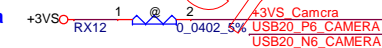
## For Camera



## Touch Screen

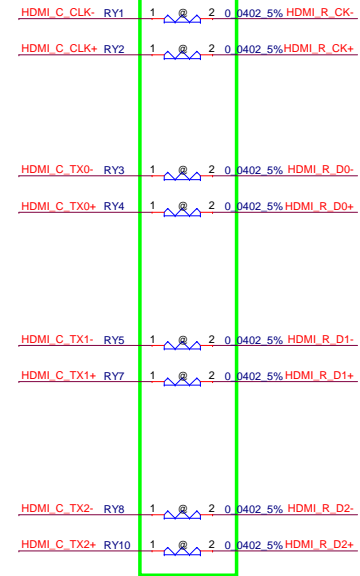
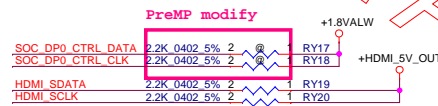
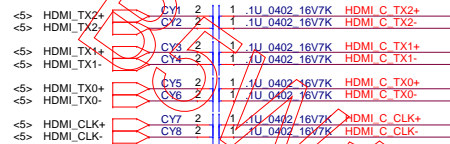
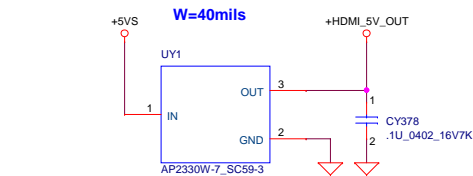
- <27> TS\_EN
- <7> USB20\_P5
- <7> USB20\_N5
- <9> I2C3\_SCL\_PNL
- <9> I2C3\_SDA\_PNL
- <27> TS\_RST#
- <24> TS\_INT#

## For Camera



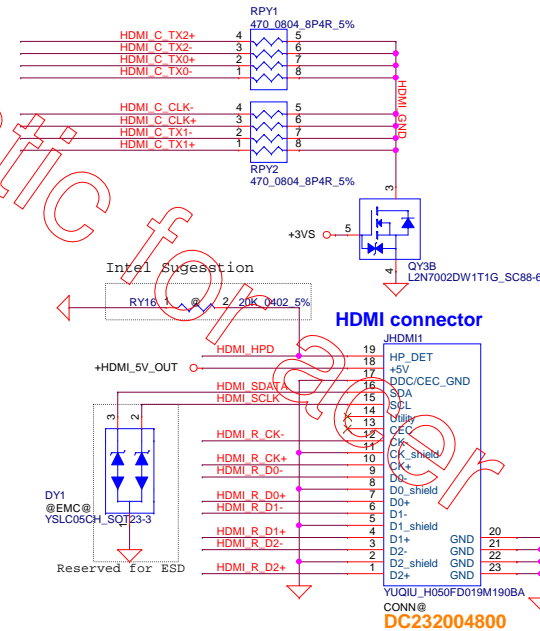
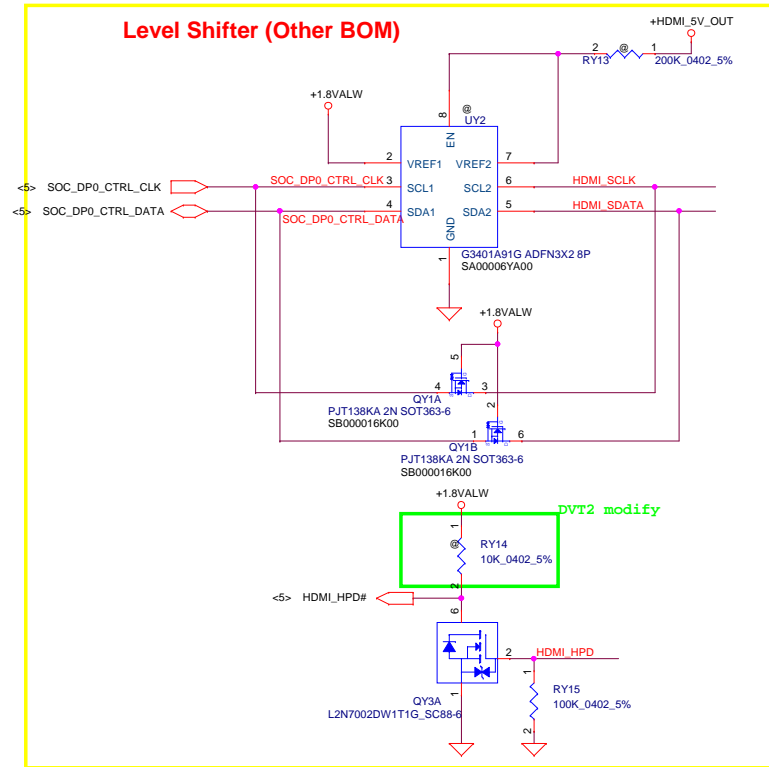
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title	
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Date: Monday, July 25, 2016		Sheet 20 of 45		Rev 1.A	





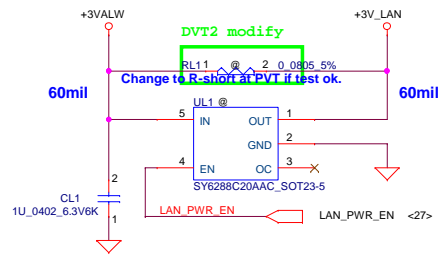
EMI 4/25 confirm OK  
DVT2 modify

### Level Shifter (Other BOM)



ZZZ1  
HDMI ROYALTY  
ROYALTY HDMI W/LOGO+HDCP  
RO000003HM  
45@

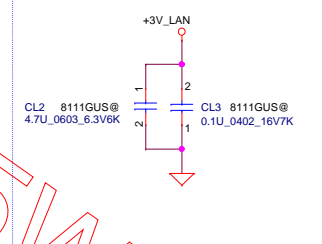
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2014/03/19		Deciphered Date		2015/03/18		Title			
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						Document Number		B5W1A LA-D641PR1A		Rev 1.A	
						Date		Monday, July 25, 2016		Sheet 21 of 45	



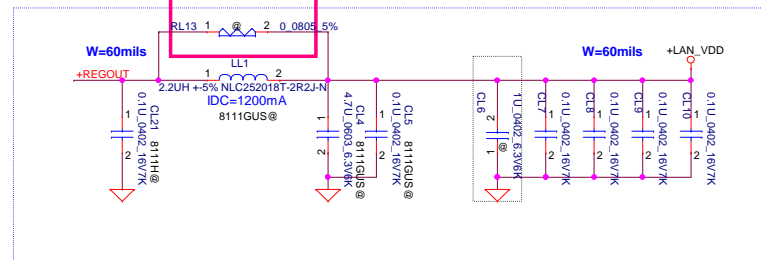
+3V\_LAN Rising time request: 0.5~100mS

SA000028Y10  
High active.  
EN threshold voltage :1.2~2.0V  
Current limit threshold :1.5~2.8A  
Output turn-on rising time: 1.3~2.7ms

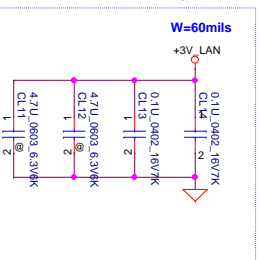
Close to U20  
Pin23



( Should be place within 200 mils )  
Close to Pin 24

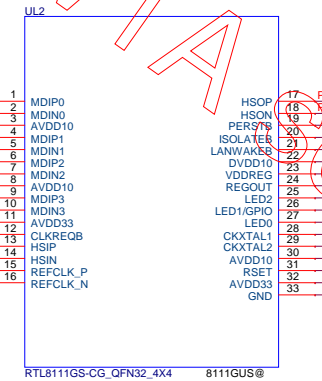
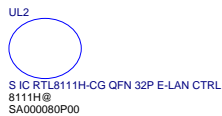


0.1uF close to Pin 11,32



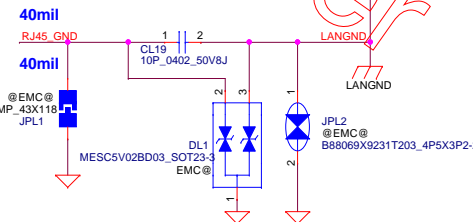
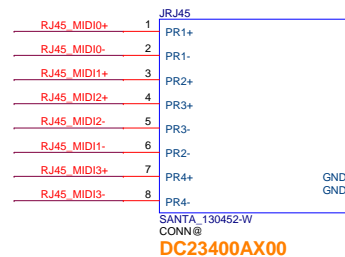
PU to +3VS at PCH  
side

<8> LAN\_CLKREQ#  
<8> PCIE\_PTX\_C\_DRX\_P2  
<8> PCIE\_PTX\_C\_DRX\_N2  
<8> CLK\_PCIE\_LAN  
<8> CLK\_PCIE\_LAN#

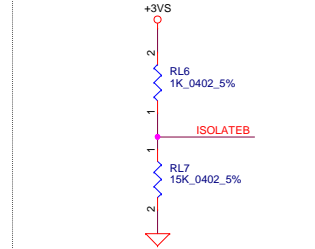


Use 8111GS symbol , pop 8111GUS part

LAN  
Connector

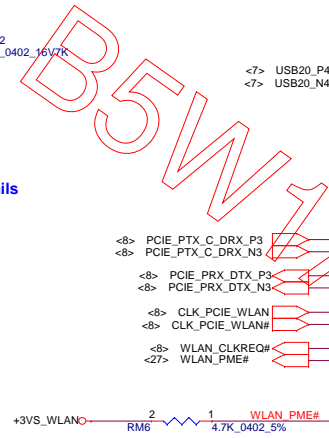
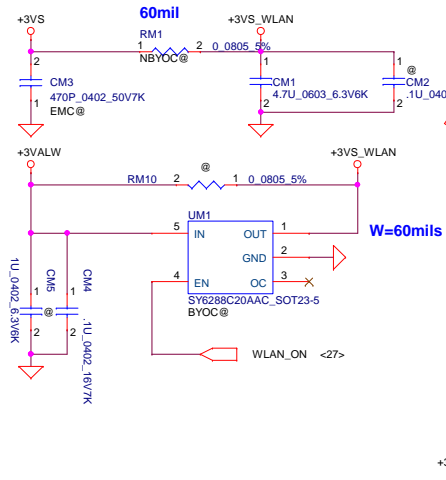


Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor RL7 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.



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LAN_RTL8111GUS-CG				1.A
B5W1A_LA-D641PR1A				Monday, July 25, 2016
Sheet 22 of 45				

# For Wireless LAN



<7> USB20\_P4  
<7> USB20\_N4

1 JNGFF1  
2 GND\_1  
3 USB\_D+  
4 USB\_D-  
5 GND\_7  
6 PCM\_CLK  
7 SDIO\_CMD  
8 SDIO\_DAT0  
9 SDIO\_DAT1  
10 SDIO\_DAT2  
11 SDIO\_DAT3  
12 SDIO\_WAKE  
13 SDIO\_RST

25 GND\_33  
26 PET\_RX\_P0  
27 PET\_RX\_N0  
28 GND\_39  
29 PER\_TX\_P0  
30 PER\_TX\_N0  
31 GND\_45  
32 REFCLK\_P0  
33 REFCLK\_N0  
34 GND\_51  
35 CLKREQ#  
36 PE\_WAKE#  
37 GND\_57  
38 I2C\_DAT  
39 I2C\_CLK  
40 RSVD\_PCIE\_RX\_P1  
41 RSVD\_PCIE\_RX\_N1  
42 RSVD\_PCIE\_TX\_P1  
43 RSVD\_PCIE\_TX\_N1  
44 RSVD\_70  
45 RSVD\_71  
46 RSVD\_72  
47 RSVD\_73  
48 RSVD\_74  
49 GND\_75

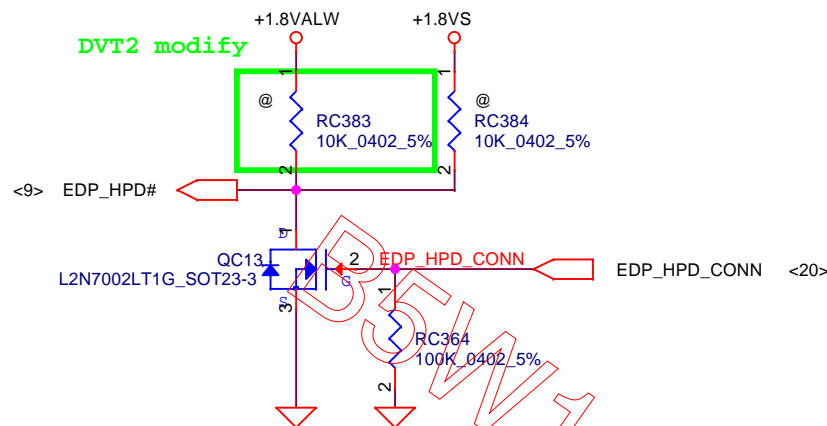
BELLW 80152-3221  
CONN#  
SP070013E00

P80CLK and BT\_ON enable separete.

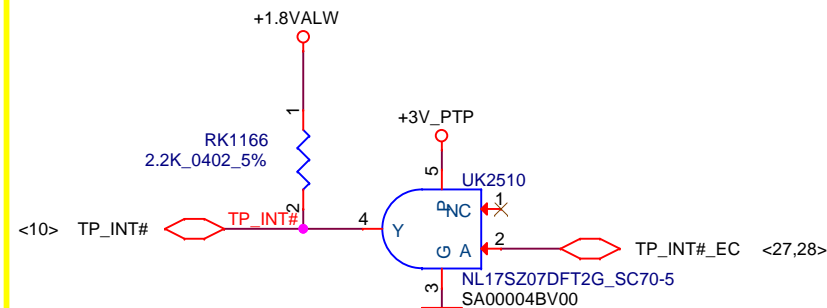
## NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKP1	73
70	UM_Power_SRC/GPIO/PEWake#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ#	GND	69
66	UM_SW_PERT#	Reserved/PERP1	67
64	RESERVED	SVIO	65
62	ALERT# (I/O/3.3)	Reserved/PET#1	63
60	DC_CLK (I/O/3.3)	Reserved/PET#1	61
58	DC_DATA (I/O/3.3)	Reserved/PET#1	59
56	VL_DISABLE# (I/O/3.3V)	GND	57
54	Reserved/V_DISABLE# (I/O/3.3V)	PEWake# (I/O/3.3V)	55
52	PERSTON (I/O/3.3V)	CLKREQ# (I/O/3.3V)	53
50	SUSCLK (33MHz) (I/O/3.3V)	GND	51
48	COEX1 (I/O/1.8V)	REFCLKN0	49
46	COEX2 (I/O/1.8V)	REFCLKP0	47
44	COEX3 (I/O/1.8V)	GND	45
42	VENDOR DEFINED	PER#0	43
40	VENDOR DEFINED	PER#0	41
38	VENDOR DEFINED	PET#0	39
36	UART_RTS (I/O/1.8V)	PET#0	37
34	UART_CTS (I/O/1.8V)	PET#0	35
32	UART_TX (I/O/1.8V)	GND	33
30	UART_RX (I/O/1.8V)	SVIO Reserve (I/O/1.8V)	31
28	UART_Wake# (I/O/3.3V)	SVIO Wake# (I/O/1.8V)	29
26	GND	SVIO DAT0 (I/O/1.8V)	27
24	LED#1 (I/O)	SVIO DAT1 (I/O/1.8V)	25
22	PCM_OUT/IS_SD_OUT (I/O/1.8V)	SVIO DAT2 (I/O/1.8V)	23
20	PCM_IN/IS_SD_IN (I/O/1.8V)	SVIO DAT3 (I/O/1.8V)	21
18	PCM_SYNC/IS_VS (I/O/1.8V)	SVIO CLK (I/O/1.8V)	19
16	PCM_CLK/IS_SCK (I/O/1.8V)	SVIO CLK (I/O/1.8V)	17
14	LED#1 (I/O)	GND	15
12	LED#1 (I/O)	GND	13
10	LED#1 (I/O)	GND	11
8	LED#1 (I/O)	GND	9
6	LED#1 (I/O)	GND	7
4	3.3V	3.3V	5
2	3.3V	GND	3

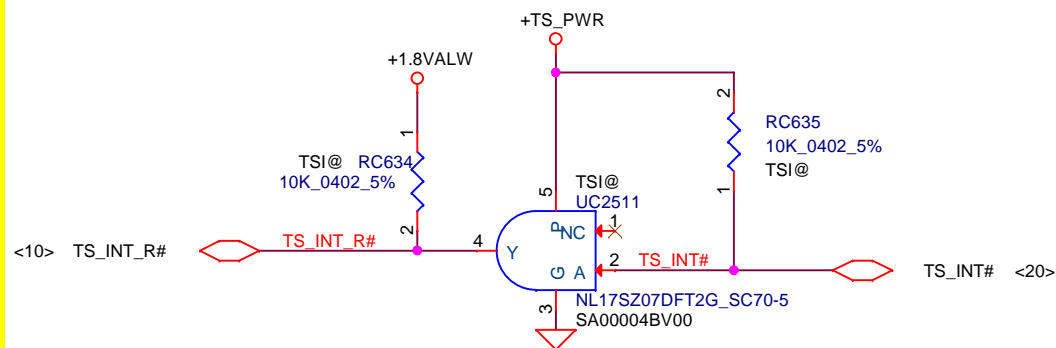
## eDP Level Shifter (Other for BOM)



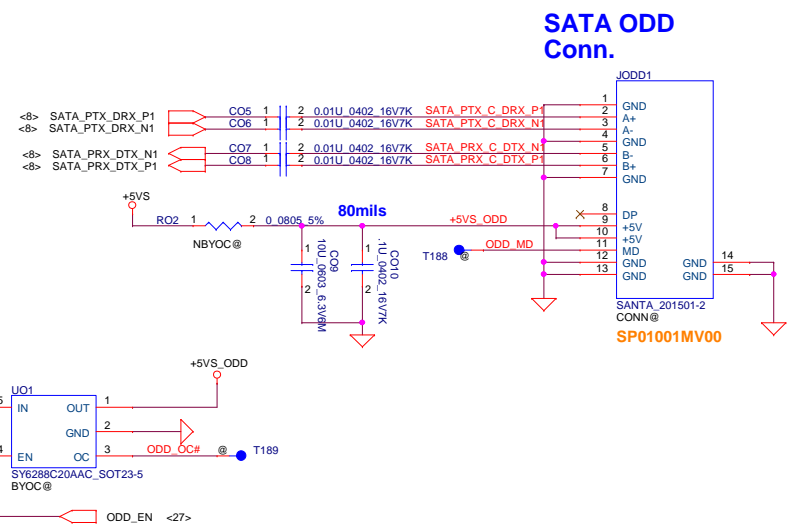
## TP\_INT Level Shifter



## TS Level Shifter (Other for BOM)

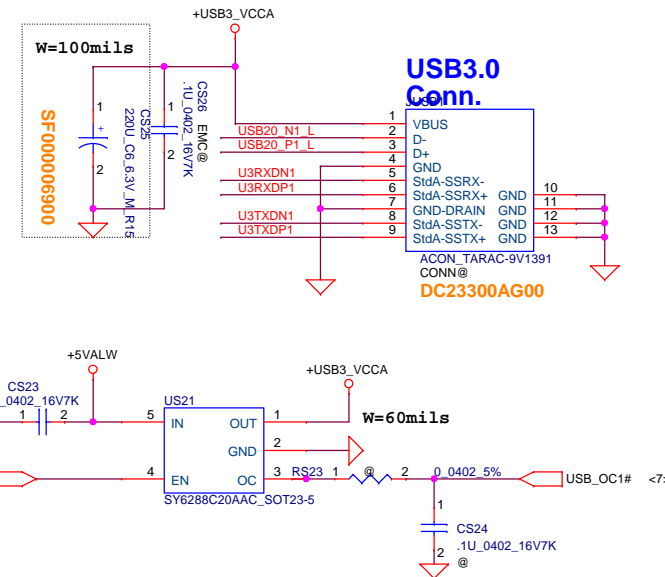
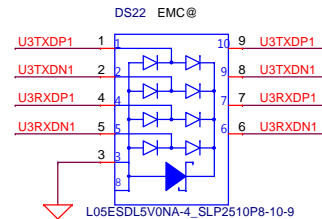
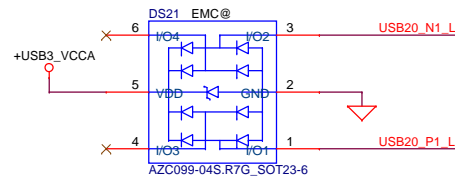
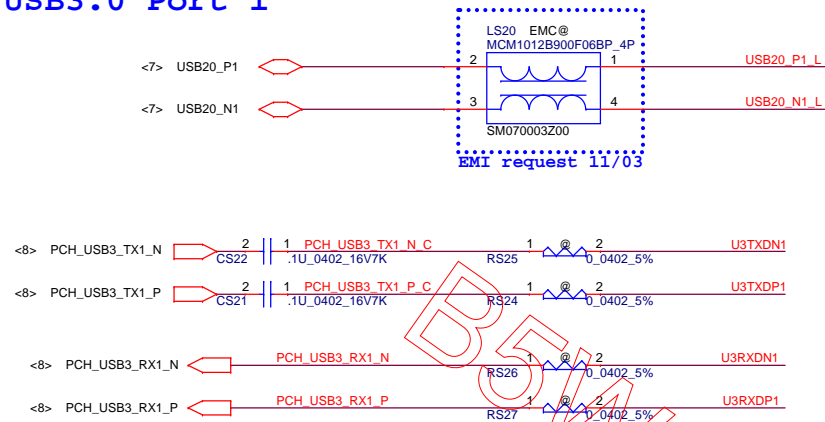


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				Size Custom	Rev 1.A
				Document Number	
				B5W1A_LA-D641PR1A	
				Date: Monday, July 25, 2016	Sheet 24 of 45

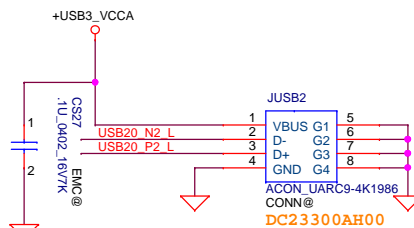
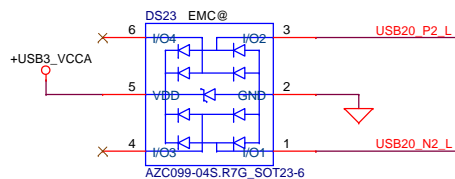
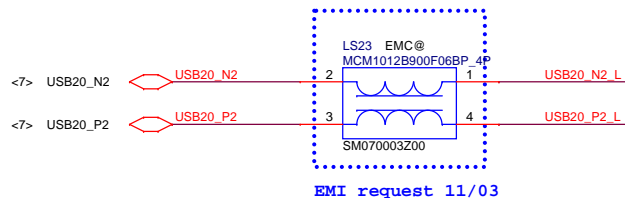


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Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title	HDD/ODD
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				B5W1A LA-D641PR1A	
Date: Monday, July 25, 2016				Sheet	25 of 45

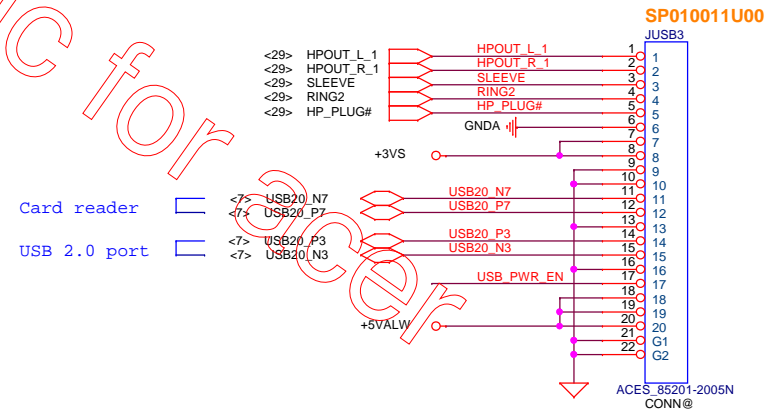
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## USB2.0 Port 2



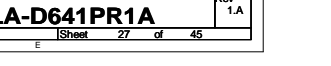
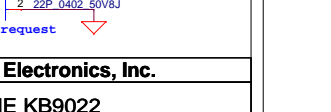
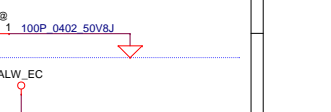
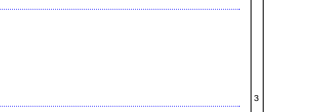
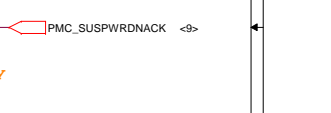
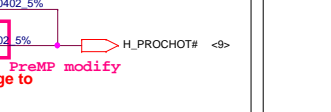
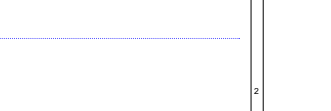
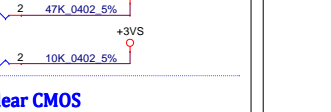
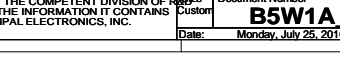
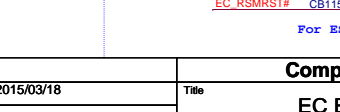
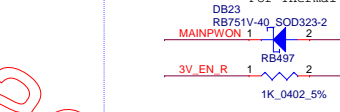
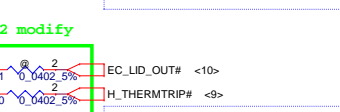
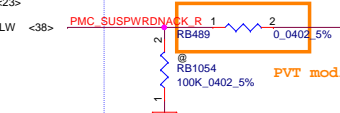
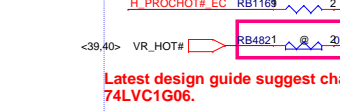
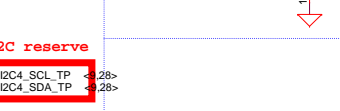
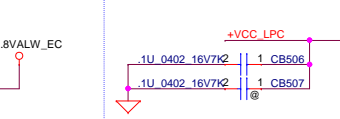
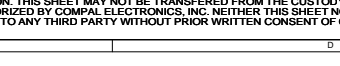
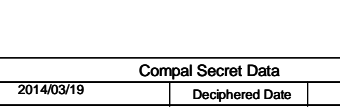
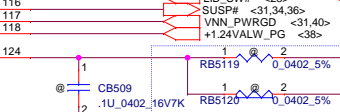
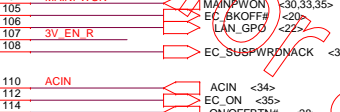
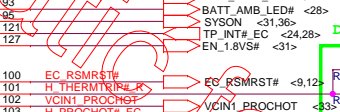
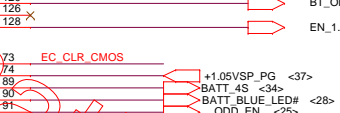
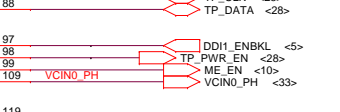
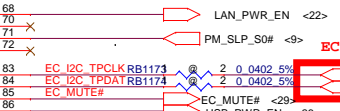
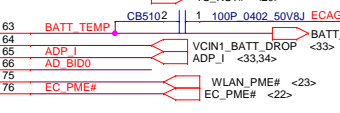
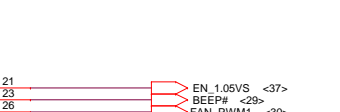
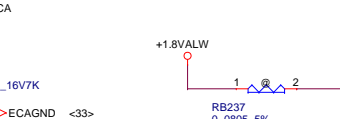
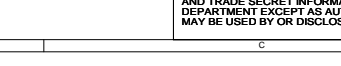
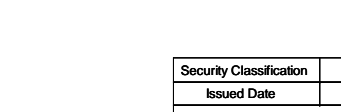
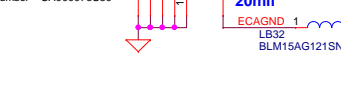
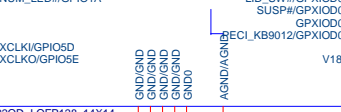
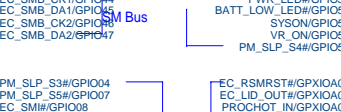
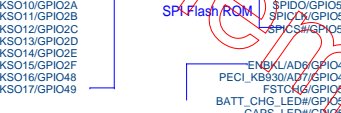
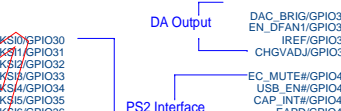
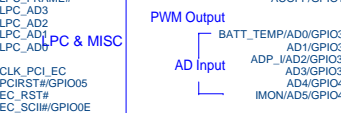
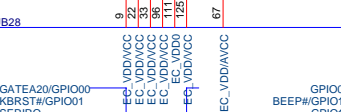
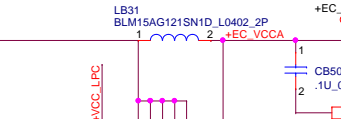
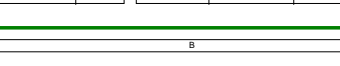
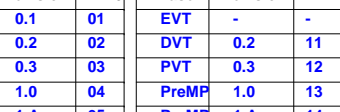
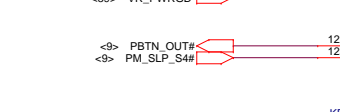
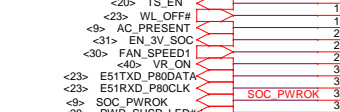
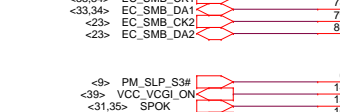
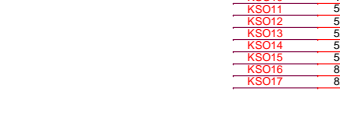
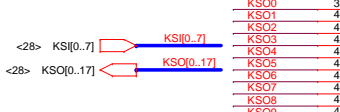
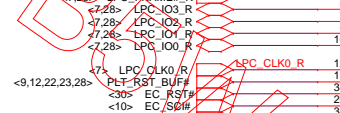
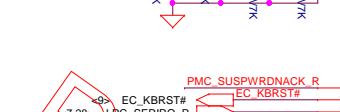
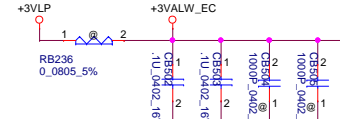
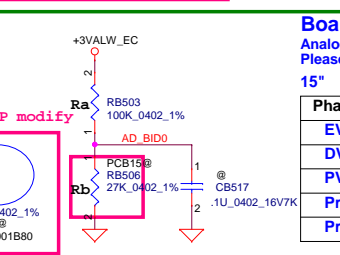
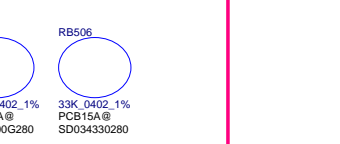
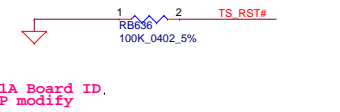
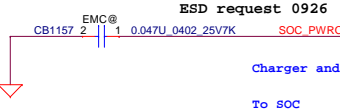
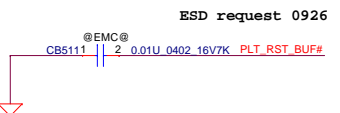
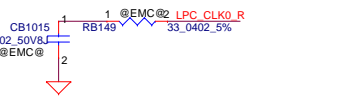
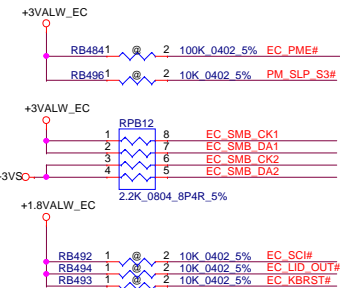
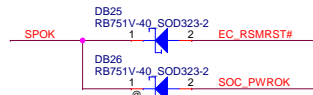
pin define need to update  
USB/B (USB, AUDIO, CR)



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Issued Date				2014/08/28				Title			
Deciphered Date				2016/08/28				USB Conn			
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				Date:				Monday, July 25, 2016			
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For abnormal shutdown



Board ID  
Analog Board ID definition,  
Please see page 3.

Phase	Revision	BID0	Phase	Revision	BID1
EVT	0.1	01	EVT	-	-
DVT	0.2	02	DVT	0.2	11
PVT	0.3	03	PVT	0.3	12
PreMP	1.0	04	PreMP	1.0	13
PreMP	1.A	05	PreMP	1.A	14

Security Classification

Compal Secret Data

Issued Date

2014/03/19

Deciphered Date

2015/03/18

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Title

Compal Electronics, Inc.

Customer

EC ENE KB9022

Document Number

B5W1A LA-D641PR1A

Date

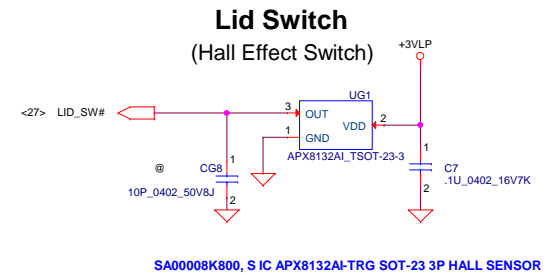
Monday, July 25, 2016

Sheet

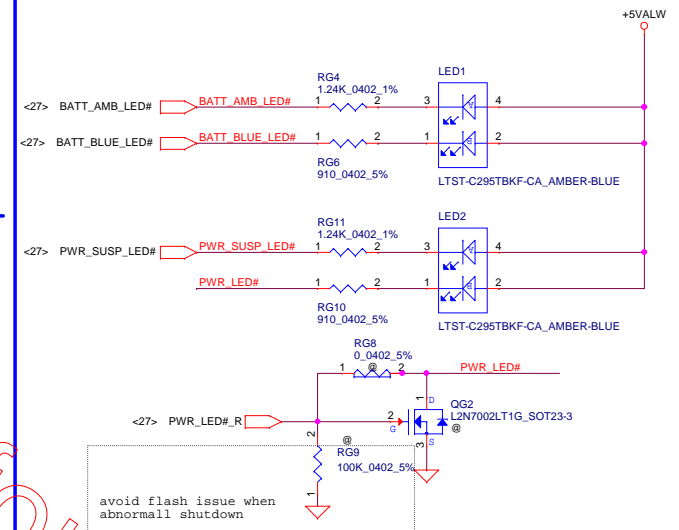
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Rev

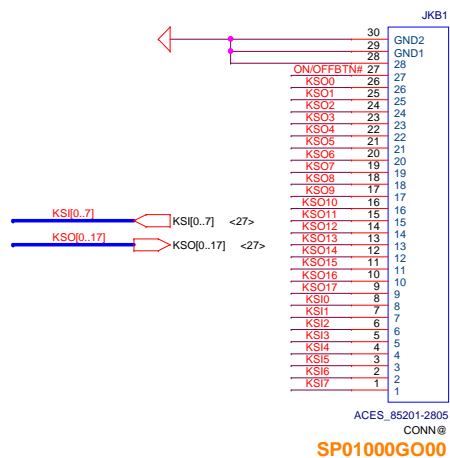
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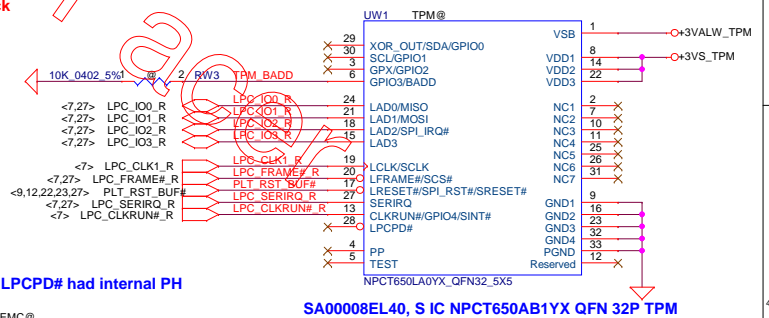
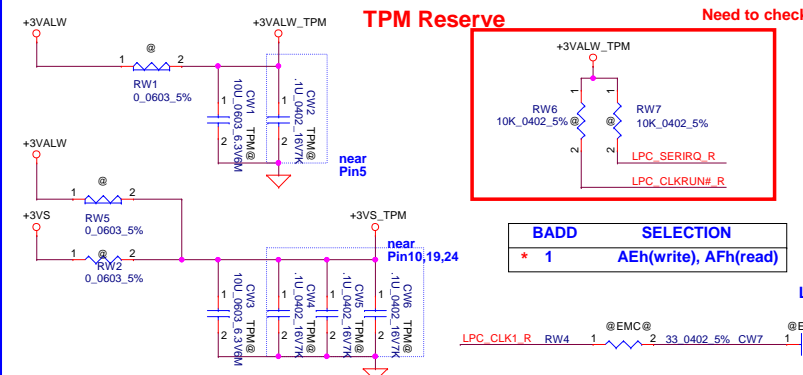
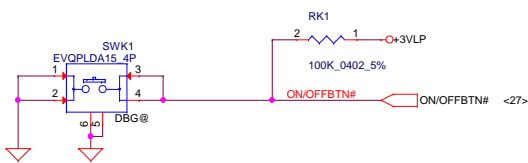
**LED**



**KB  
Conn.**



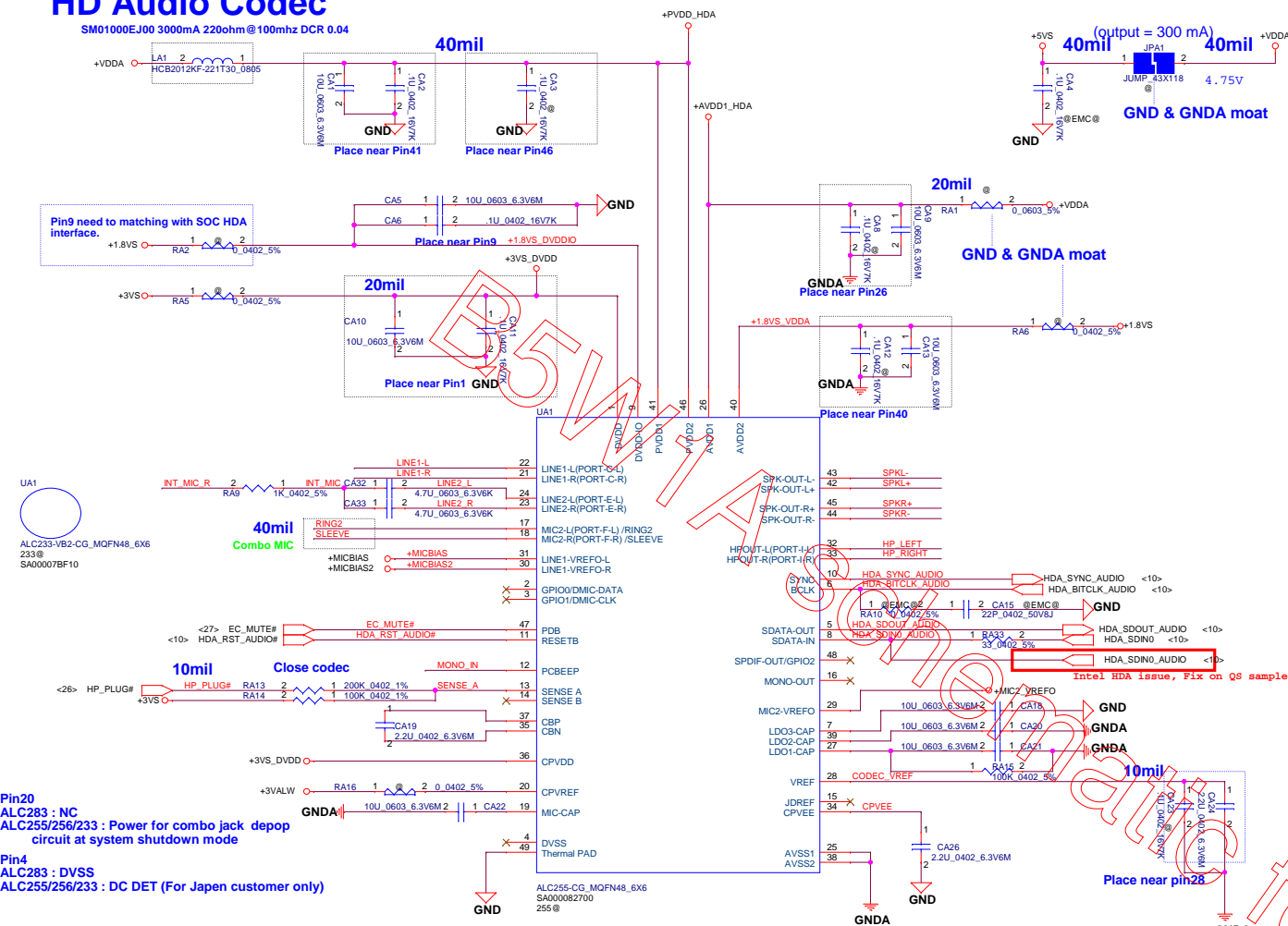
ON/OFF BTN  
Test only



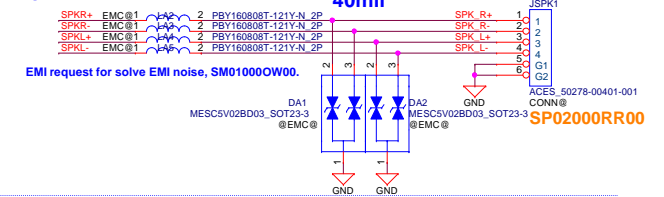
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Issued Date	2014/03/19	Deciphered Date	2015/03/18	Title	KB/TP/LED/TPM / Hall sensor
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				Custom <b>B5W1A LA-D641PR1A</b>	1.A
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# HD Audio Codec

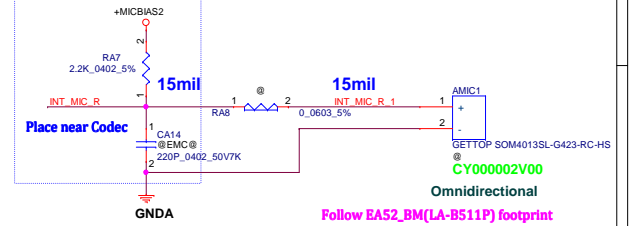
SM01000EJ00 3000mA 220ohm@100mhz DCR 0.04



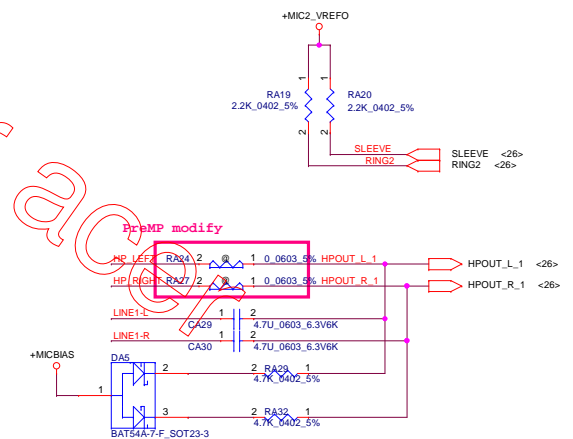
## Int. Speaker Conn.



## Analog MIC(SMD)



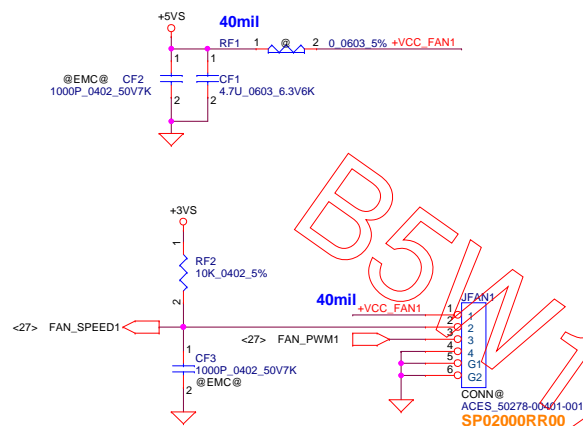
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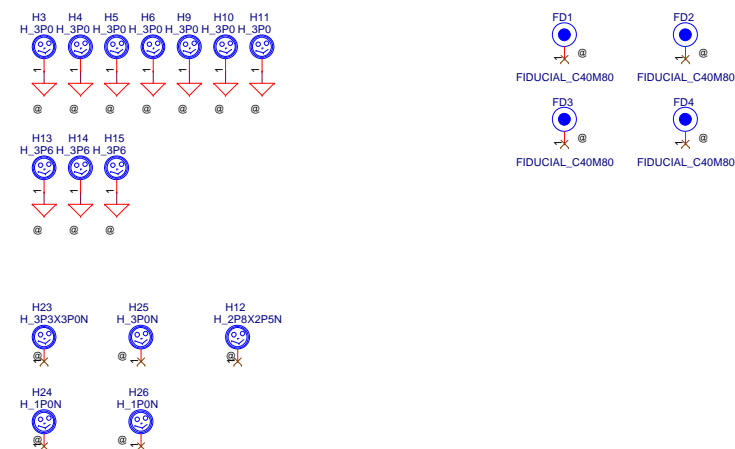
Pin15  
ALC283 : Ref. Resistor for Jack Detect  
ALC255/256/233 : Jack Detect for SPDIF-OUT and SPK-OUT port

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2015/10/02		Deciphered Date		2016/11/10		Title		HD Audio Codec ALC255/ALC233 Colay	
Size		Custom		Document Number		B5W1A LA-D641P1A		Rev		1.A	
Date		Monday, July 25, 2016		Sheet		29		of		45	

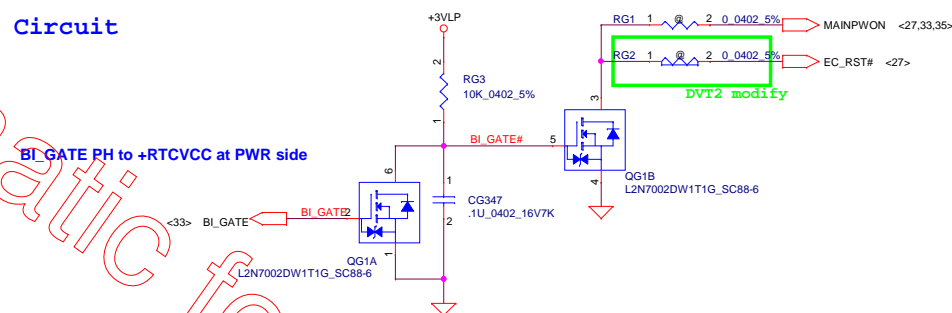
## FAN1 Conn



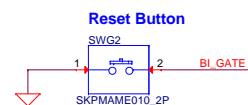
## Screw Hole



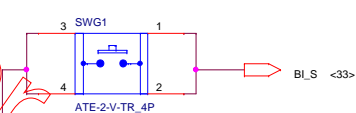
## Reset Circuit



## Reset Button

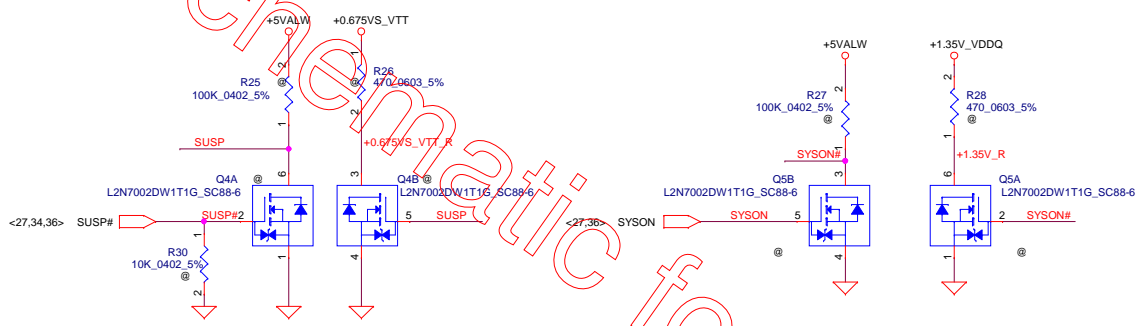
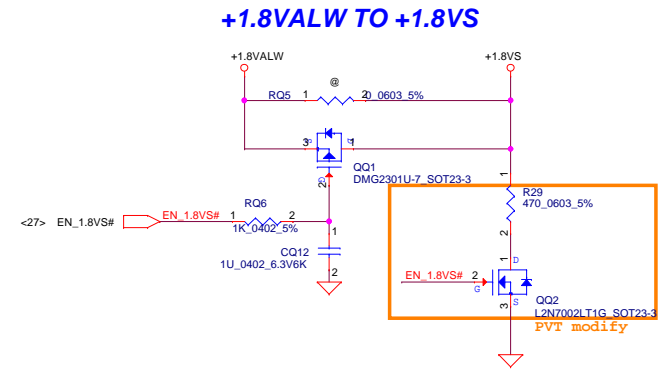
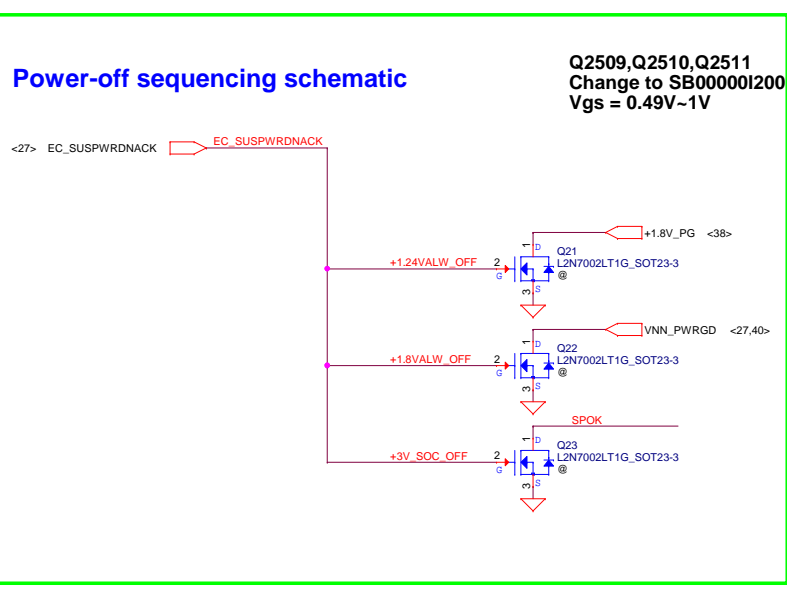
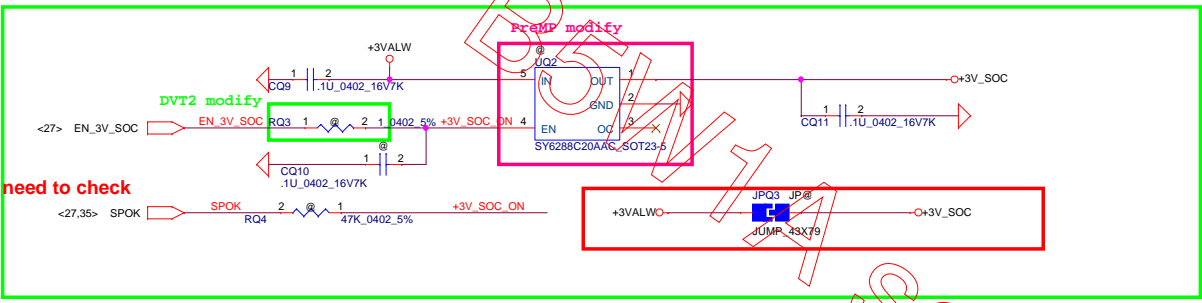
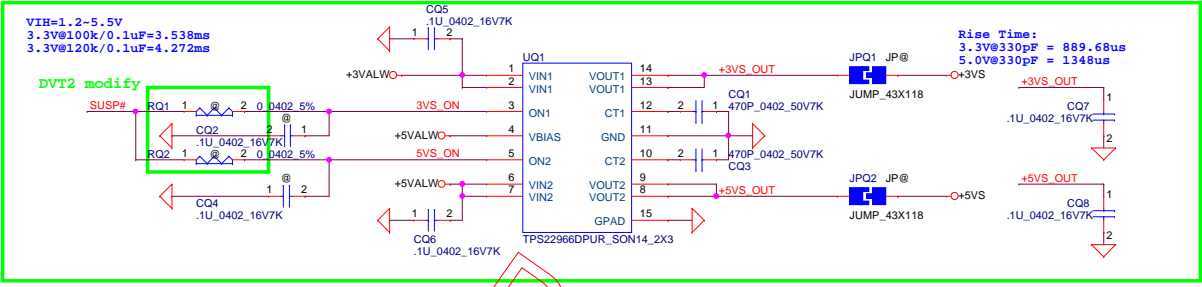


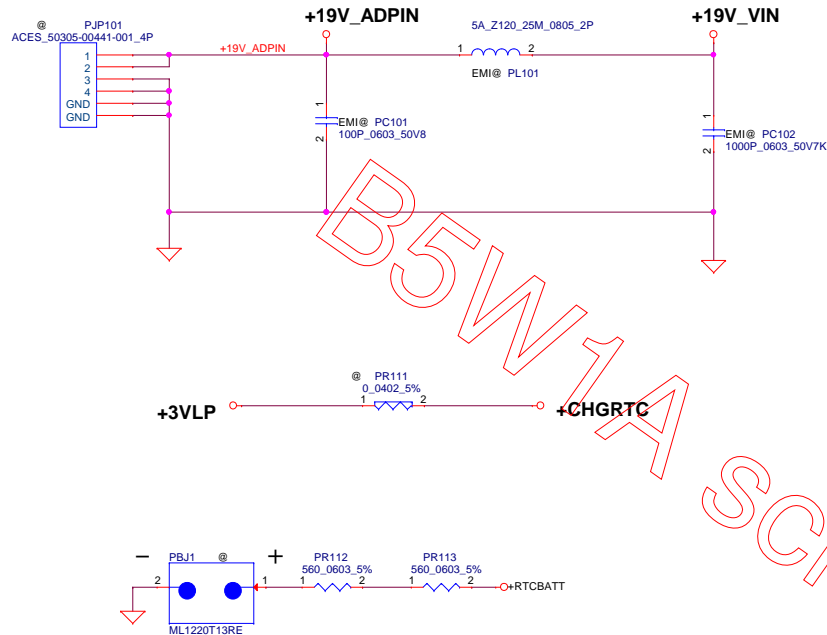
## BI SW



**Release : Battery Off**  
**Push : Battery ON**

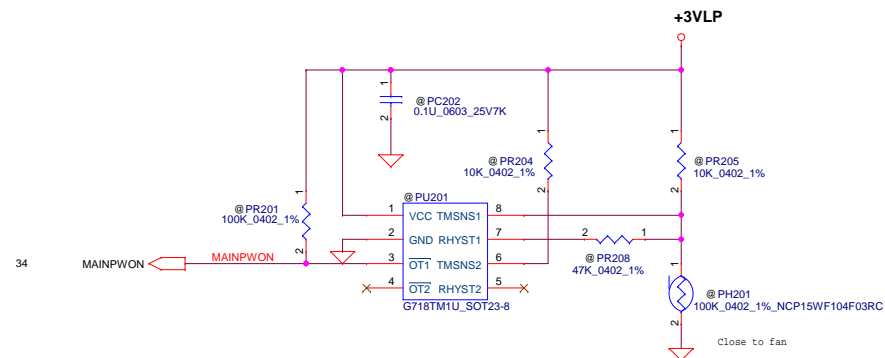
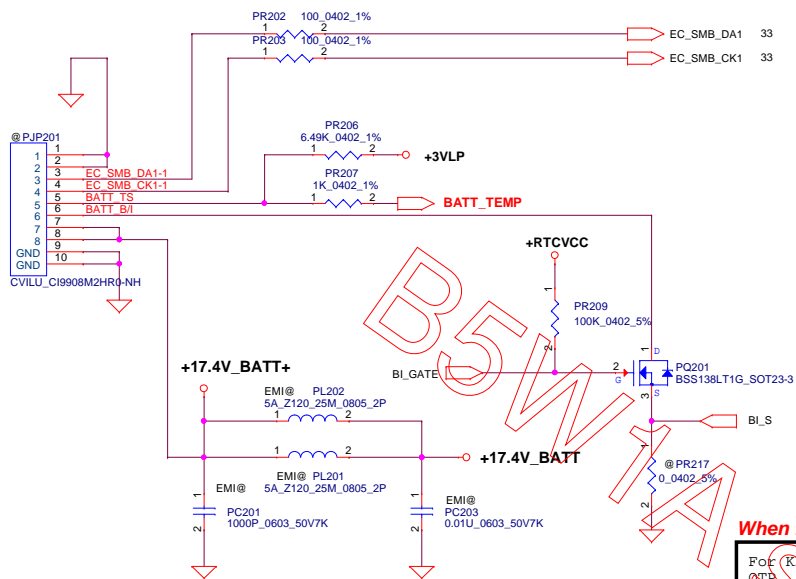
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Issued Date		2014/08/28	Deciphered Date		2016/08/28	
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				FAN & Screw Hole & Reset Button		
				Document Number		
				BSWIA LA-D641PRIA		Rev 1/
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When PR210=16.9K

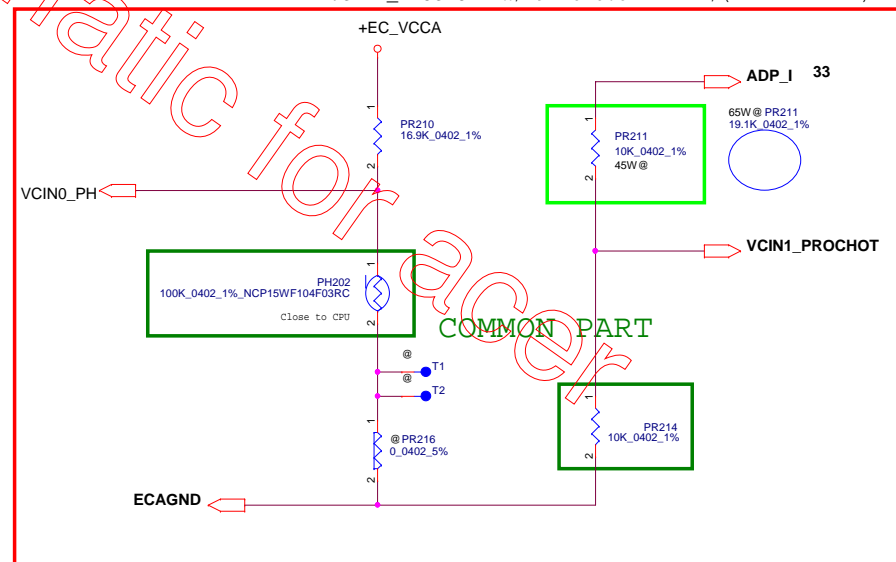
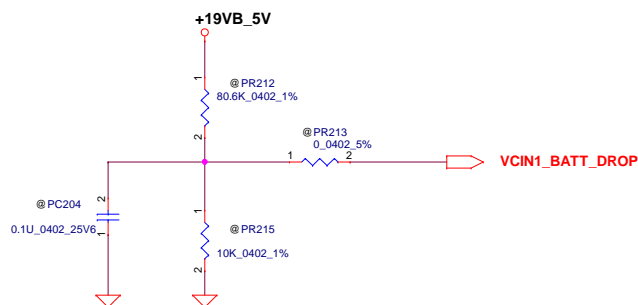
For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92°C, 1V	56°C, 2V
PH202 (ohm)	7.3092K	26.11K

2015/09/30 update

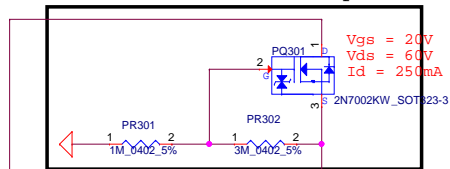
VCIN1_PROCHOT For KB9022 sense 20mΩ	Active	Recovery	PR211
65W	84.5W, 0.61V	84.5W, 0.61V	19.1KΩ SD034191280
45W	58.5W, 0.61V	58.5W, 0.61V	10KΩ SD034100280

130% 130%

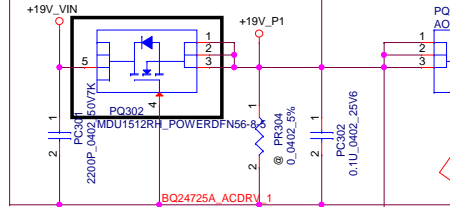
$$VCIN1\_PROCHOT = PW / 19 * 20 * 0.02 * PR214 / (PR211 + PR214)$$



# Protection for reverse input

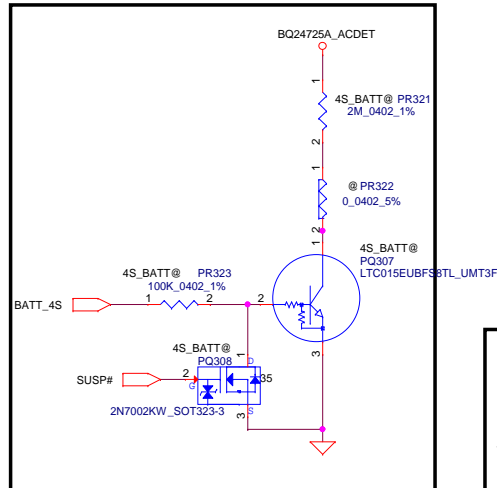


Need check the SOA for inrush



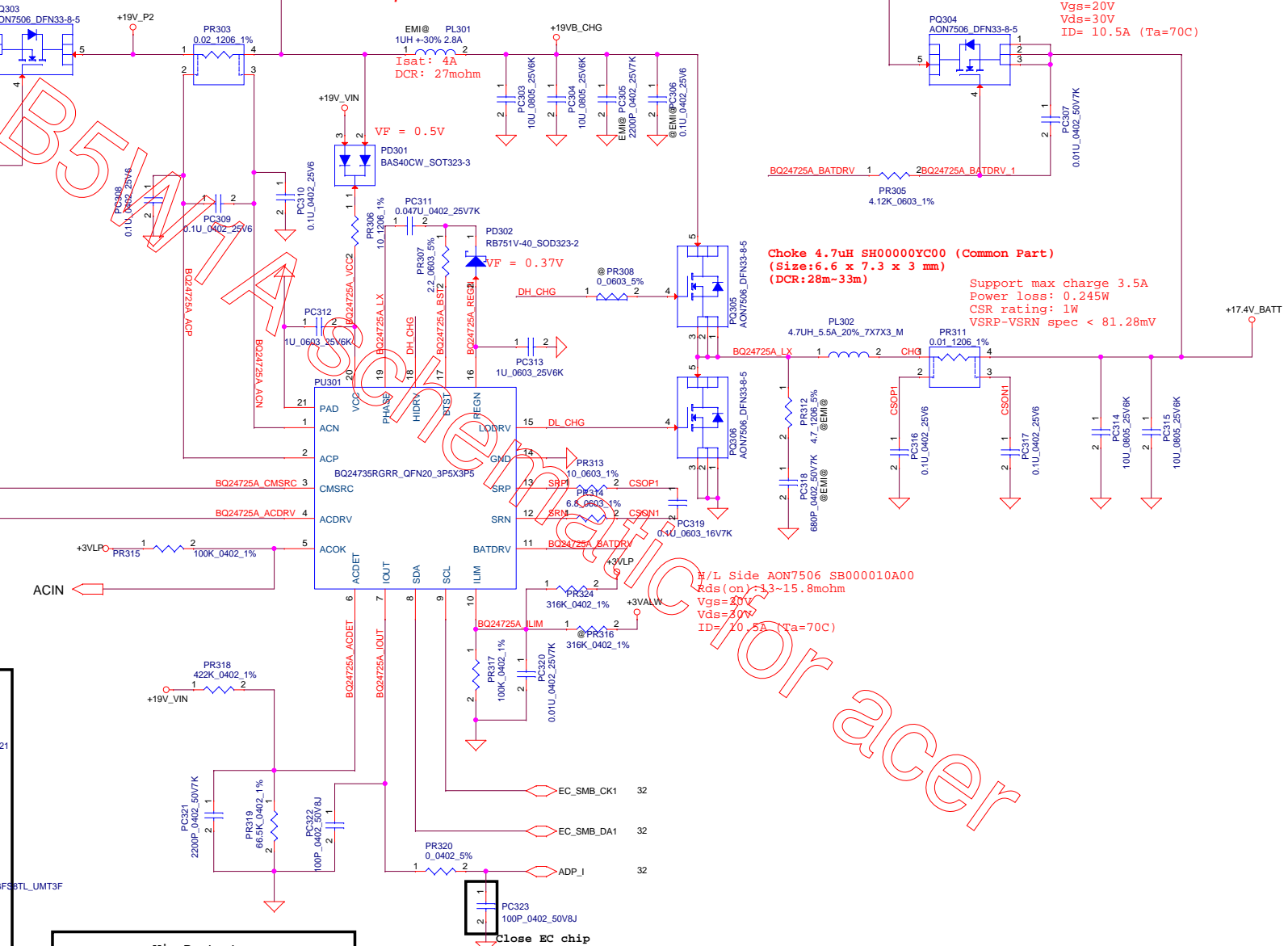
ACFET MDU1512 SB00000SY00  
Rds(on): 4.2~5mohm  
Vgs=20V  
Vds=30V  
ID= 24.2A (Ta=70C)

For 4S per cell 4.35V battery



RBFET AON7506 SB000010A00  
Rds(on): 13~15.8mohm  
Vgs=20V  
Vds=30V  
ID= 10.5A (Ta=70C)

2014/01/21 update PL301 change  
Common part SH00000YG00



## Vin Detector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

$$VILIM = 20 * ILIM * Rsr$$

$$ILIM = 3.3 * 100 / (100 + 316) / 20 / 0.01$$

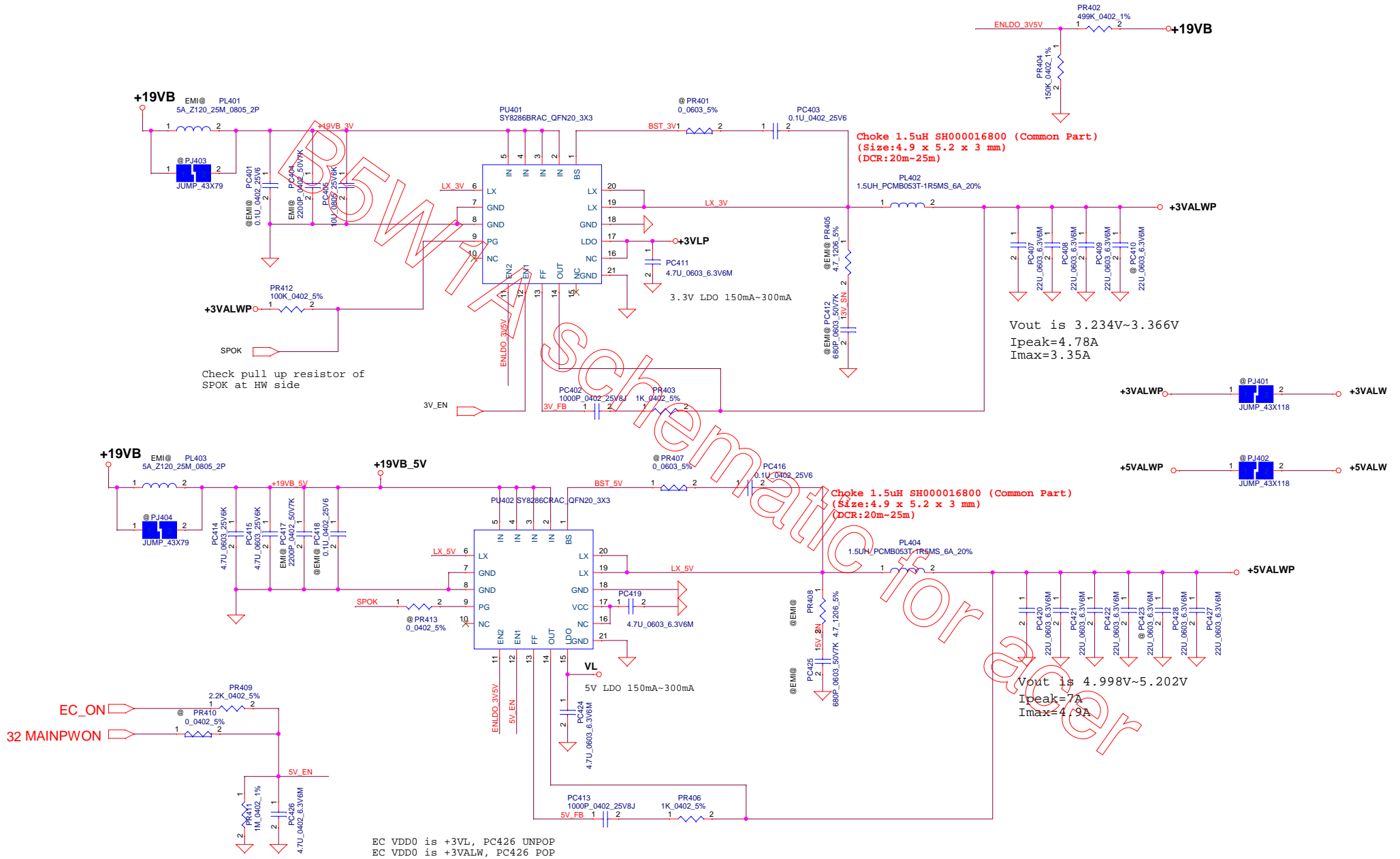
$$= 3.966 A$$

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Issued Date	2013/10/01	Deciphered Date	2014/05/24
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CHARGER

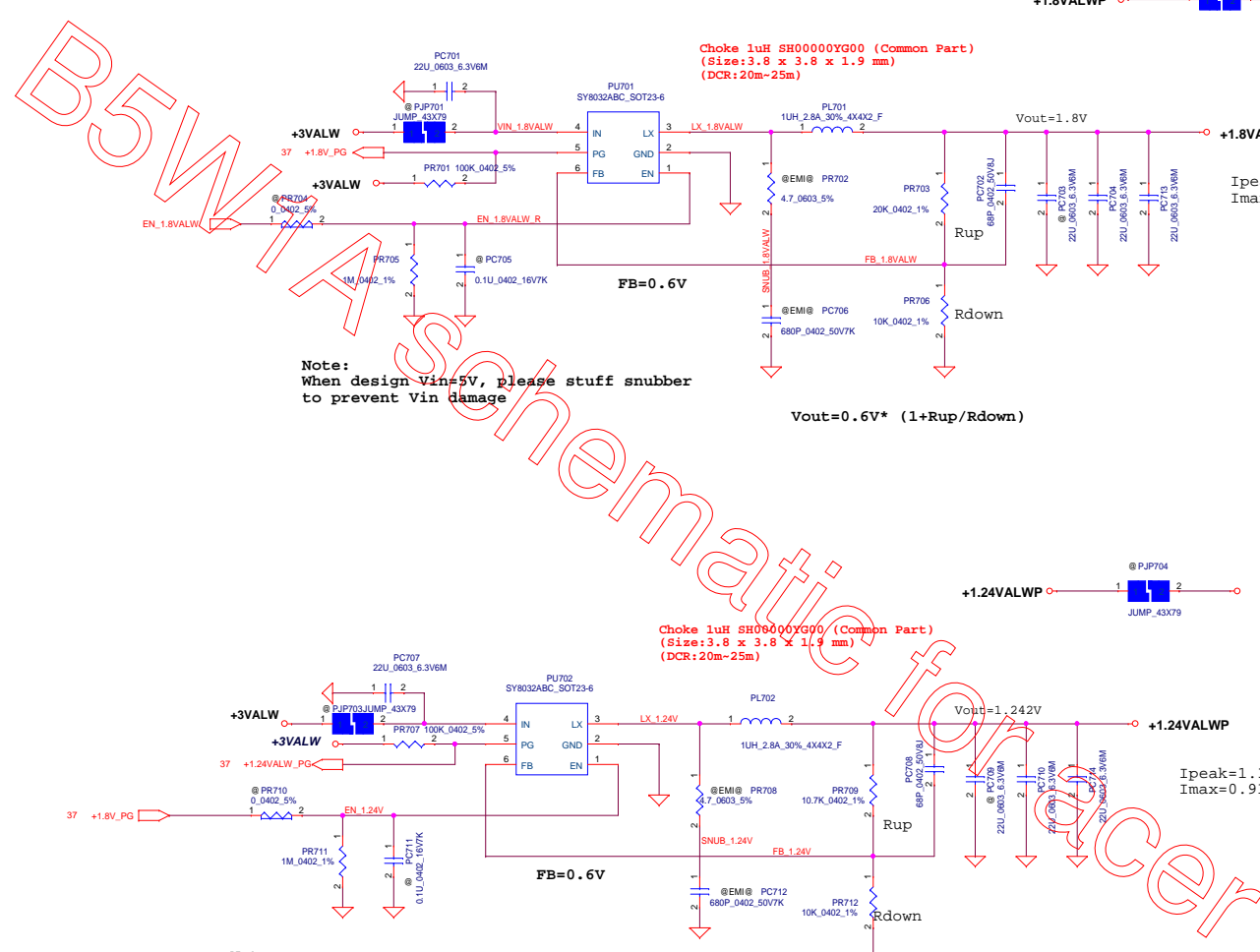
Size	Document Number	Rev
	Common Circuit	1.A
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Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	3VALW/5VALW
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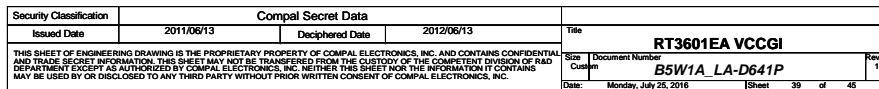
Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

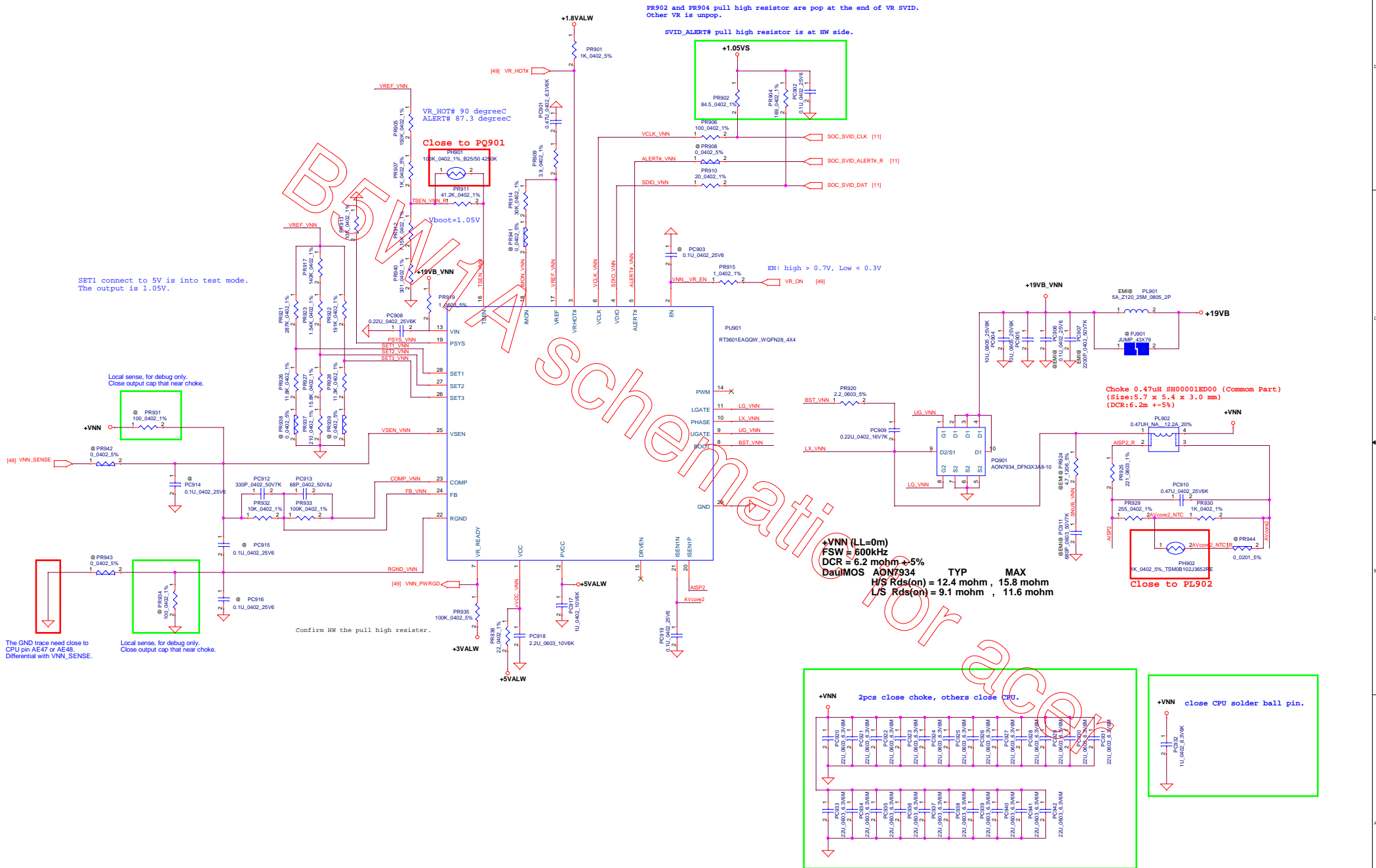
Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

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Issued Date		2011/06/13	Deciphered Date	2012/06/13	Title
					SY8032
					Size C Document Number
					B5W1A_LA-D641P
					Rev 1.A
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SET1 connect to 5V is into test mode.  
The output is 1.05V.





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Issued Date	2011/06/13	Deciphered Date	2012/06/13	RT3601EA VNN	
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				Rev	1A

## Version change list (P.I.R. List)

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for PWR

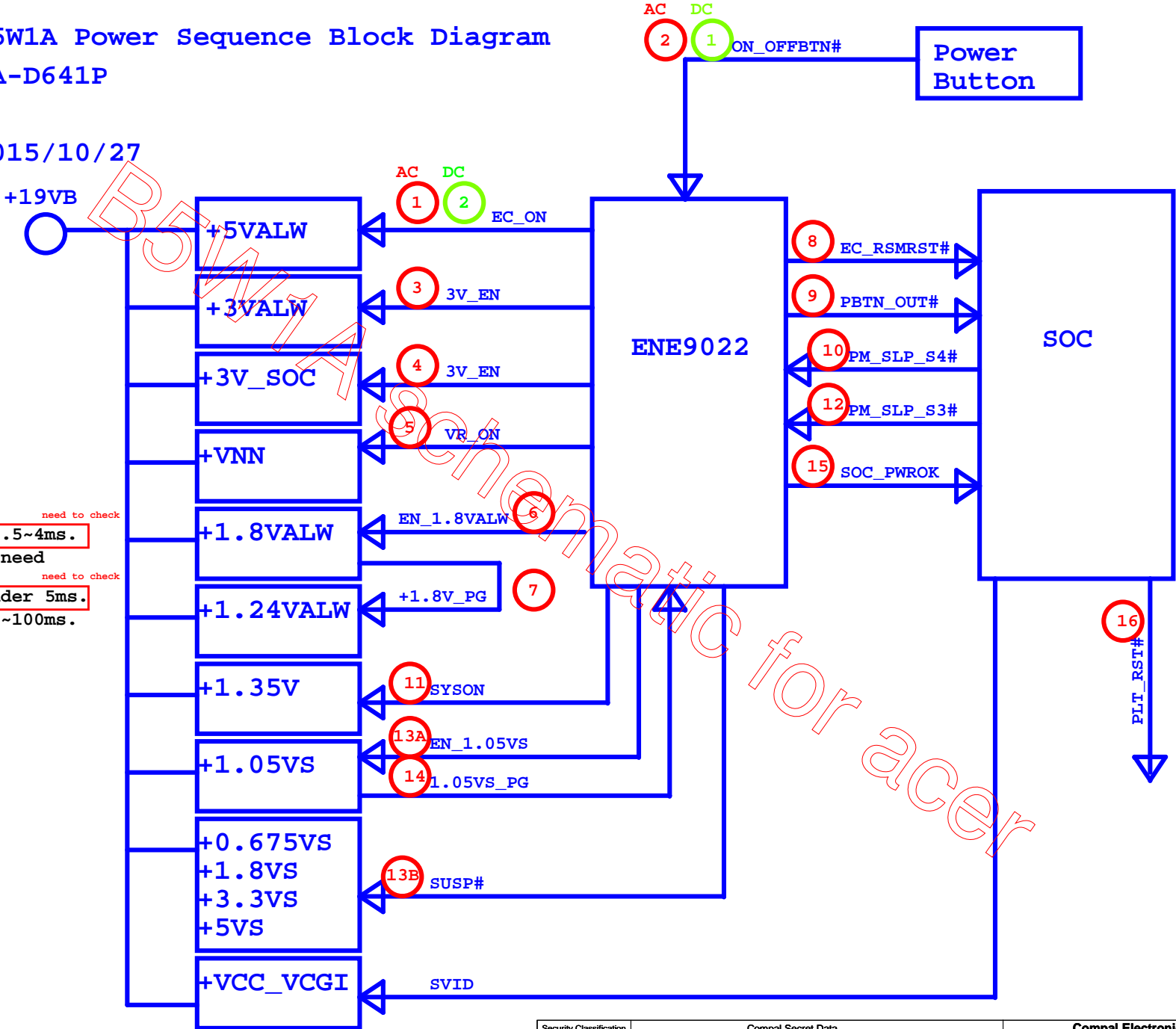
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design update	Solution Change	01	34	Change the PQ305 from MDV1528 to AON7506. Change the PQ306 from MDV1527 to AON7506.	12/01	EVT
2	Design update	Power Sequence Modify	02	40	Change the PR935.2 from connect +1.8VALW to +3VALW.	12/11	DVT
3	Design update	Solution Change	02	34	Change the PL302 from 10uF to 4.7uF.	12/15	DVT
4	Design update	Solution Change	02	39	Change the PC803, PC804, PC805, PC806 from 4.7uF_0603 *4 to 10uF_0805 *3.	12/15	DVT
5	Design update	Power Sequence Modify	02	38	Change the PR704.2 net name from VNN_PWRGD to EN_1.8VALW. Add the PR707.2 page symbol +1.24VALW_PG.	12/28	DVT
6	Design update	CPU transient test result	02	39	Change the PC814 from 270pF to 470pF. Change the PR833 from 40.2k Ohm to 45.3k Ohm. Change the PR828 from 604 Ohm to 750 Ohm. Change the PR830 from 243 Ohm to 300 Ohm. Change the PR813 from 68.1k Ohm to 57.6k Ohm. Change the PC856 to un-pop.	12/31	DVT
7	Design update	Solution Change	02	39	Delete the jump PJ801.	12/31	DVT
8	Design update	Change the P/N to comment part	02	39	Change the PL802 P/N from SH00001D900 to SH00001EE00.	01/05	DVT
9	Design update	Solution Change	02	35	Change the PR401 from 0 Ohm to R-short. Change the PR407 from 0 Ohm to R-short.	01/28	DVT
10	Design update	Cancel Co-lay	03	34,39	Delete the jump PJ301 and capacitance PC857.	04/25	DVT-2
11	Design update	Solution Change	03	36,37 38,39	Change the PR509, PR601, PR704, PR710, PR815 from 1 Ohm to R-short.	04/25	DVT-2
12	Design update	Solution Change	03	39,40	Change the PR842, PR843, PR807, PR942, PR943, PR908 from 0 Ohm to R-short.	04/28	DVT-2
13	Design update	Solution Change	03	40	Change the PC930, PC931 from 0402 1uF to 0603 22uF.	04/28	DVT-2
14	Design update	Solution Change	03	40	Change the PC924, PC929, PC931, PC933, PC939 from un-pop to pop for PVT test.	04/28	DVT-2
15	Design update	CPU transient test result	03	40	Change the PC913 from 39pF to 68pF. Change the PR933 from 100k Ohm to 60.4k Ohm. Change the PR925 from 191 Ohm to 221 Ohm. Change the PR929 from 232 Ohm to 255 Ohm. Change the PR914 from 21.5k Ohm to 35.7k Ohm. Change the PL902 from 0.68uH to 0.47uH.	05/04	DVT-2
16	Design update	Solution Change	1.0	40	Change the PR942 from R-short to 0 Ohm.	05/17	Pre MP
17	Design update	ME red ink result	1.0	36	Add PC520, PC521, PC522 to on-pup, and change PC512, PC513, PC515 to un-pop.	06/20	Pre MP
18	Design update	CPU transient test result	1.0	40	Change the PR914 from 35.7k Ohm to 30k Ohm. Change the PR933 from 60.4k Ohm to 100k Ohm.	07/07	Pre MP
19	Design update	Solution Change	1.0	39,40	Change the PR841, PR938, PR939, PR941, PR942 from 0 Ohm to R-short.	07/07	Pre MP

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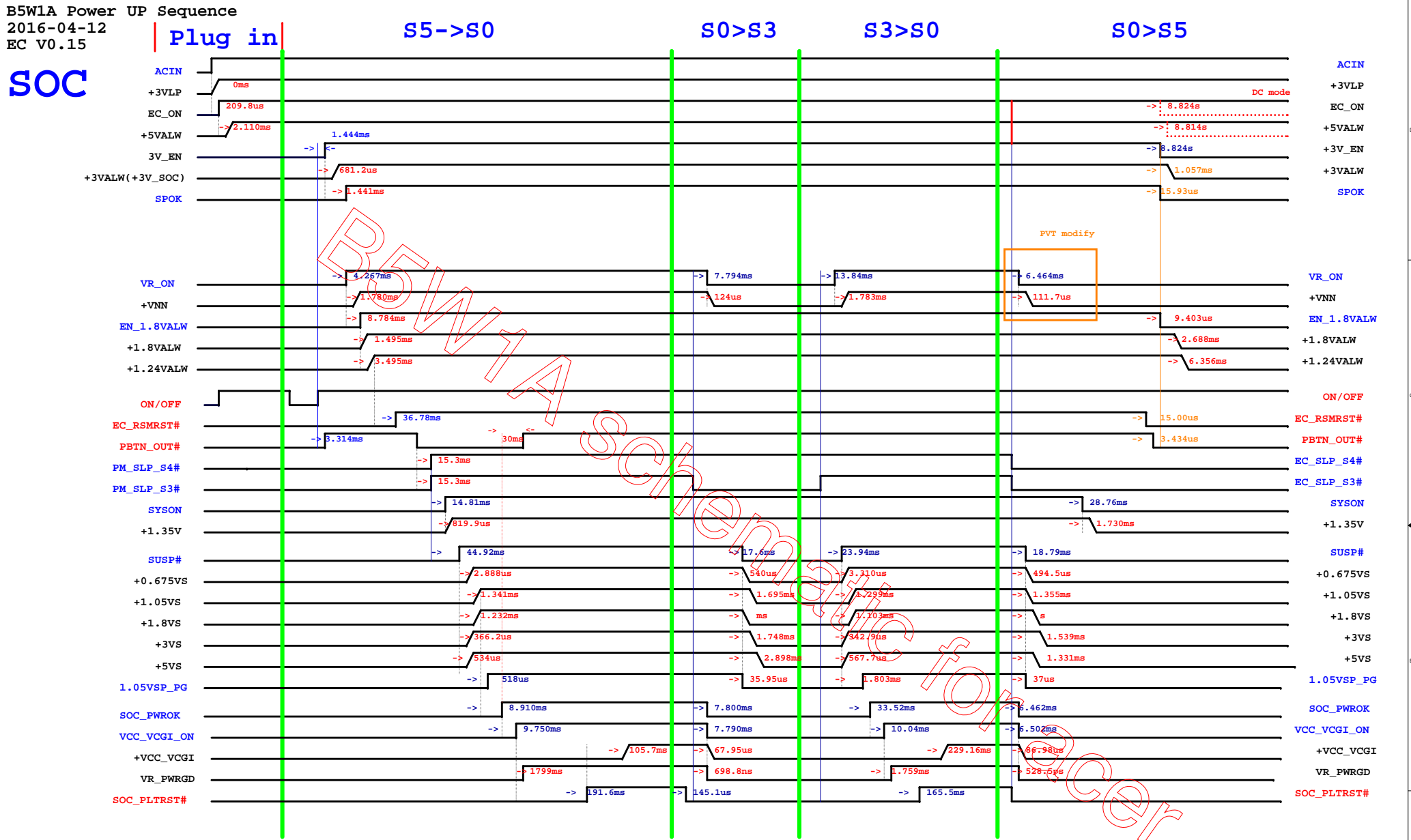
# COMPAL CONFIDENTIAL

MODEL NAME: B5W1A Power Sequence Block Diagram  
PCB NAME: LA-D641P  
REVISION:  
DATE: 2015/10/27

Note:  
1.7 to 8 need over 10ms  
(compal setting 30ms)  
2.10 to 11 need under 2.5~4ms.  
3.+0.675VS rising time need  
under 100us.  
4.12 to +1.05VS need under 5ms.  
5.14 to 15 need set 5ms~100ms.  
(compal setting 20ms)



SOC



## Version change list (P.I.R. List)

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for HW

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design update	Remove SOC side ODD_EN	0.2	P.09	only need reserve EC side ODD_EN	12/28	DVT
2	Design update	UC56 need PU to +3VS	0.2	P.09	Remove RC492 and add RC1162	12/28	DVT
3	Design update	GPIO43 need to PD	0.2	P.11	RC408 un-stuff, pop RC433	12/28	DVT
4	Design update	Diode may cause leakage	0.2	P.19	D1 un-stuff, pop U2	12/28	DVT
5	Design update	reserve VNN_PWRGD(Pin117) & +1.24VALW_PG(Pin118)	0.2	P.27	reserve only	12/28	DVT
6	Design update	for power sequence control +1.8VALW	0.2	P.27	add EC pin EN_1.8VALW	12/28	DVT
7	Design update	for EC Board ID	0.2	P.27	change RB506 to 15K	12/28	DVT
8	Design update	Change speaker bead PN by sourcer request.	0.2	P.29	Change LA2,LA3,LA4,LA5 PN from SM01000CC00 to SM01000OW00.	12/28	DVT
9	Design update	for 1.8VS discharge	0.2	P.31	add R29,QQ2	12/28	DVT
10	Design update	for 1.8VS soft start	0.2	P.31	pop CQ12	12/28	DVT
11	Design update	Reserve PD and follow EVT SMT BOM	0.2	P.09	Reserve RC492 and pop RC99	12/29	DVT
12	Design update	For cost reievew	0.2	P.21	Remove RY11,RY12,QY2	12/29	DVT
13	Design update	DFX highlight EM5209VF_DFN14_3X2 footprint symbol dosen't release	0.2	P.31	change UQ1 footprint to TPS22966DPUR_SON14_2X3	12/29	DVT
14	Design update	For enlarge H13-15 Screw GND pad to avoid thermal module scrape to PCB	0.2	P.30	change Screw hole from 4.2mm to 3.6mm	01/05	DVT
15	Design update	follow memory down white paper	0.2	P.17	change RD154,RD155 to 1K	01/08	DVT
16	Design update	follow vendor's suggestion	0.2	P.07	change CC7,CC137 to 15pF	01/08	DVT
17	Design update	follow vendor's suggestion	0.2	P.12	change CC15,CC16 to 15pF	01/08	DVT
18	Design update	For part count	0.2	P.20	RX10,RX11 change to R short	01/22	DVT
19	Design update	For cost down experiment	0.2	P.09	change RC524,RC525,RC528,RC529 location for QC2511 & QC2508 cost down	01/22	DVT
20	Design update	For HDMI part count	0.2	P.21	change RY1-5,RY7,RY8,RY10 to 1ohm	01/22	DVT
21	Design update	Follow intel checklist	0.2	P.09	Remove RPC27,add RC342-344 for PM_RST_BTN# need to PU 2.7K	01/22	DVT
22	Design update	For 0 ohm part count	0.2	P.09, P.28	RG8,RC213,RC211 change to R short	01/22	DVT
23	Design update	For common component	0.2	P.07,21 30,31	SB000000DH00 change to SB000000PV00	01/22	DVT
24	Design update	For common component	0.2	P.18	change SE000000G880 to SE076104K80(CD48,50,51,54,58)	01/22	DVT
25	Design update	For intel suggestion	0.2	P09,27	H_THERMTRIP# connect to EC pin 126	01/22	DVT
26	Design update	For I2C cost down	0.2	P.09	unpop QC2508,pop RC528,RC529	01/28	DVT
27	Design update	For DVT phase part count reduce	0.2	P.26	USB3 CMC change to R short (Del LS21-LS22,add RS24-27)	01/28	DVT
28	Design update	For common part	0.2	P.30	change CF1 SE000000MA00 to SE107475K80 (10V change to 6.3V)	01/29	DVT
29	Design update	for H_THERMTRIP# reserve	0.2	P.27	reserve RB490	01/29	DVT
30	Design update	For correct to ABO material	0.2	P.12	change 105_0402_1% from SD00000FY8L to SD00000FY00	01/29	DVT
31	Design update	For DVT phase	0.2	P.05	change CPU PN for ES2 QKKW(SA00009S800),QKKX(SA00009S900), QKKY(SA00009SA00)	02/02	DVT
32	Design update	For Intel 2016 WW04 Sightings Report update(560733)	0.2	P.10	Change RC79 from 1K_0402_1% to 680_0402_1%	02/02	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
33	Design update	For different Fan table	0.2	P.27	Add 17" EC board ID	02/02	DVT
34	Design update	for 1.8VS discharge	0.3	P.31	QQ2 change to Q4B, and stuff Q4 & R25, un stuff QQ2	04/12	DVT2
35	Design update	verify +3V_SOC for cost down	0.3	P.31	Un stuff RQ3 as DVT memo	04/12	DVT2
36	Design update	For intel request	0.3	P.27	change H_THERMTRIP# to EC pin 101	04/12	DVT2
37	Design update	follow CRB	0.3	P.9	SOC_PLTRST# reserve PU +3VS change to +3V_SOC	04/12	DVT2
38	Design update	for BOM structure option	0.3	P.16	change memory down BOM structure to MD@	04/12	DVT2
39	Design update	for part count reduce.	0.3	P.21	HDMI RY1~RY5,RY7~RY8,RY10 change to R short	04/25	DVT2
40	Design update	Intel HDA issue, Fix on QS sample.	0.3	P.10	RC4983&RC779 un-stuff	04/25	DVT2
41	Design update	Follow APL PDG v1.2 suggestion	0.3	P.7	Del RPC28, add RC522,RC524,RC525,RC516	04/25	DVT2
42	Design update	Follow APL Checklist v1.2 suggestion	0.3	P.24	un stuff RC383, and BIOS internal PU	04/25	DVT2
43	Design update	Follow APL Checklist v1.2 suggestion	0.3	P.21	un stuff RY14, and BIOS internal PU	04/25	DVT2
44	Design update	For 0 ohm part count reduce	0.3	P9 10 22 23	RL1,RC99,RC528,RC529,RC1052,RG2	04/25	DVT2
45	Design update	For part count reduce	0.3	P.31	RQ1,RQ2 change from 1ohm to RShort	04/25	DVT2
46	Design update	for option SM Bus	0.3	P.18	reserve RD168 to PU +3VALW	04/26	DVT2
47	Design update	for part count reduce	0.3	P.18	RD165 change to 0ohm	04/26	DVT2
48	Design update	intel checklist v1.2 update	0.3	P.9	RC344 change from 2.7K to 10K	04/26	DVT2
49	Design update	Update DVT2 Board ID	0.3	P.27	RB506 change to 20K(15") and 200K(17")	04/26	DVT2
50	Design update	Connect PMC_SUSPWRDNACK from SOC to EC	0.3	P.27	Stuff RB489	05/12	PVT
51	Design update	Update circuit	0.3	P.5	Update QS CPU in circuit	05/24	PVT
52	Design update	add +1.8VS discharge circuit	0.3	P.31	stuff R29 & QQ2	05/24	PVT
53	Design update	Update Pre MP Board ID	1.0	P.27	change EC board ID 15" to 27K,17" to 240K	06/27	PreMP
54	Design update	PDG 1.5 update	1.0	P.21	RY17&RY18 un stuff	06/27	PreMP
55	Design update	RC517,RC519,RC480,RC481,RC476,RC145,RC146,RD165,RL13,RB482 chagne to RS	1.0	P.7,13,14 18,22,24	for 0 ohm part count reduce	06/27	PreMP
56	Design update	For ME EN	1.0	P.10	RC1052 change to 0ohm	06/27	PreMP
57	Design update	For part count reduce	1.0	P.31	UQ2 un stuff	06/27	PreMP
58	Design update	For intel PDG update	1.0	P.12	swap JCMOS1 & JCMOS2,SOC_SRTCRST# & SOC_RTCTEST#	07/04	PreMP
59	Design update	For part count reduce	1.0	P.13	RC476 & RC481 change to 0_0603	07/04	PreMP
60	Design update	For +1.35V power	1.0	P.14	add RC147 for +1.35V R short	07/05	PreMP
61	Design update	For 0 ohm part count reduce	1.0	P.29	change RA24,RA27 to R short	07/05	PreMP
62	Design update	For part count reduce	1.0	P.12	RC340 & RC402 change to @CMC@	07/05	PreMP
63	Design update	For MP BOM	1.A	P.05	Update B0 & B1 CPU	07/22	PreMP
64	Design update	For intel spec update	1.A	P.12	un stuff RC273,RC266,RC268	07/22	PreMP
65	Design update	For intel spec update	1.A	P.12	change RC245,RC93 to 57.6K stuff RC251	07/22	PreMP
66	Design update	For PCB update	1.A	P.27	Add 1A board ID	07/22	PreMP
67	Design update	For Acer request	1.A	P.11	Add Micron on board RAM	07/22	PreMP
68	Design update	For intel signting	1.A	P.9	Un stuff RC343	07/22	PreMP

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				B5W1A LA-D641PR1A	1.A
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